International Journal of Engineering Science and Advanced Technology (IJESAT)
Vol 26 Issue 04(April),2026
Received: 18-02-2026 Accepted: 23-03-2026 Published: 01-04-2026

Low Power Delay Controlled ALU Employing CNTFET Technology

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Abstract— A key component of microprocessors, the Arithmetic and Logic Unit (ALU) is in charge of carrying out all arithmetic and logic operations necessary for computing. The design and performance study of a unique 4-bit reconfigurable ALU utilizing Carbon Nanotube Field-Effect Transistor (CNTFET) technology for improved efficiency in Very Large-Scale Integration (VLSI) systems are presented in this work. The proposed work focuses on optimizing crucial submodules like the XOR gate, 2x1 multiplexer, and 4x1 multiplexer at the transistor level using hybrid logic techniques in order to overcome the drawbacks of conventional CMOS-based ALUs, which suffer from high power dissipation, propagation delay, and area constraints. The suggested ALU greatly reduces the number of transistors and increases efficiency while maintaining the architectural benefits of a delay-controlled reconfigurable ALU. HSPICE is used to implement and simulate the design on 32 nm CNTFET technology. Significant improvements in power consumption, propagation delay, Power Delay Product (PDP), and Energy Delay Product (EDP) are shown by performance evaluation. Compared to current designs, the Suggested approach reduces the number of transistors by around 27%, improving area efficiency. The suggested ALU offers complete rail-to-rail voltage swing, lower latency, and increased energy efficiency, according to simulation findings. As a result, the design is ideal for next-generation low-power, high-performance VLSI applications, especially in IoT-based and portable systems.

Keywords—Low Power ALU, Delay-Controlled ALU, Hybrid Logic Design, Multiplexer Optimization, Reconfigurable ALU, HSPICE Simulation, Power Delay Product (PDP), Energy Delay Product (EDP)

I. INTRODUCTION

Any Central Processing Unit (CPU) or microprocessor's primary working component, the Arithmetic and Logic Unit (ALU), performs all required arithmetic and logical operations. Addition, subtraction, multiplication, division, and logical operations like AND, OR, and NOT are all carried out by this digital circuit [1]. ALUs are a crucial part that significantly affects the functioning and performance of modern computer systems since they are widely used in Very Large-Scale Integration (VLSI) systems like microcontrollers, digital signal processors (DSPs), and real-time integrated circuits. Since the speed and efficiency of the ALU directly affect data processing capacity, design optimization is still a prominent focus of research in digital electronics.

The relevance of low-power VLSI circuit design in modern electronic systems has increased, especially with the growth of portable devices and the Internet of Things (IoT). Despite being widely used in integrated circuit design, traditional complementary metal-oxide semiconductor (CMOS) technology faces challenges such increased power dissipation and propagation delay as device dimensions decrease. In submicron and deep-submicron technologies, where both static and dynamic power consumption should be minimized, these issues become much more important [2]. The primary source of dynamic power consumption is switching activity in logic gates, whereas static power

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consumption is caused by leakage currents. These characteristics have a direct impact on battery life, thermal management, and the overall durability of electronic equipment [3]. Both battery life and power consumption are significant design restrictions since many DSP applications are intended for portable devices [4]. The reduction in dynamic power consumption is the main factor that improves energy efficiency in mathematical building blocks. Static power consumption increases significantly as a result of increased leakage current across discrete devices made in VLSI ICs. Reducing both static and dynamic power consumption is essential to developing an energy-efficient ALU cell. The examination of power dissipation in CMOS-based circuitry that follows amply demonstrates this [5],[6]. As a result, major research efforts are being directed into designing energy-efficient circuit topologies and design approaches that minimize total power consumption while maintaining performance. Voltage scaling, clock gating, power gating, and subthreshold operation are popular techniques used to achieve ultra-low power operation in current VLSI systems [3], [7].

Carbon Nanotube Field Effect Transistor (CNTFET) technology is now recognized as a potential alternative for traditional CMOS devices in the next generation of nano electronic circuits. CNTFETs have benefits such as high carrier mobility, low power consumption, and the ability to modify threshold voltage by varying the dimension of the carbon nanotube. This unique feature makes it possible to create efficient digital circuits that make the best use of transistors, Because of this, CNTFET-built arithmetic circuits can achieve lower transistor counts, shorter delays, and higher power efficiency, all of which are essential for high-performance computing applications [8].

Integrating CNTFET technology into complex circuits like Arithmetic Logic Units has the ability to greatly improve performance while reducing power consumption. This improvement facilitates the development of high-speed, low-power, and compact VLSI systems, making CNTFET-based ALU design a promising path for future energy-efficient computing architectures [9].

II. Existing System-I

A number of basic building pieces that carry out both arithmetic and logical operations make up the Arithmetic and Logic Unit (ALU). As seen in Fig. 1, the ALU is implemented in this architecture employing crucial modules such as an adder, subtractor, AND gate, OR gate, and a 4x1 multiplexer (MUX). Each module is in charge of a particular function, and when combined, they allow the ALU to carry out a wide range of calculations effectively [10].

The arithmetic operations are carried out using the adder and subtractor circuits, while logical operations are performed using basic logic gates like AND and OR. The selection of desired operation is controlled by the 4x1 multiplexer, which chooses the appropriate output based on the select inputs.

The existing systems for designing Arithmetic and Logic Units (ALUs) are primarily based on conventional CMOS technology and standard logic design techniques [11].

In most of the existing designs, arithmetic operations are performed using Ripple Carry Adders (RCA), while subtraction is achieved through two's complement methods.

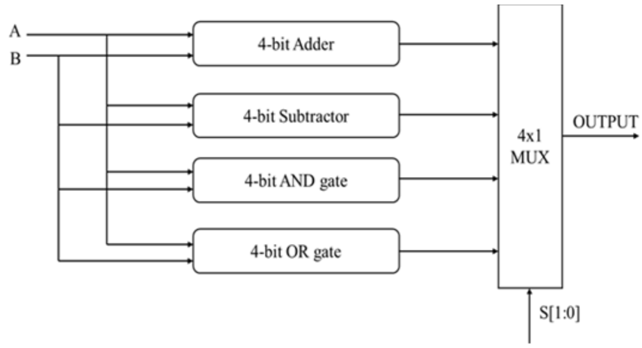

Fig. 1. Existing delay controllable 4-bit ALU [14].

TABLE I. OPERATIONS RELATED TO ALU [14]

Selection Inputs	Function
00	Addition
01	Subtraction
10	AND gate
11	OR gate

A. ADDER

A Ripple Carry Adder is a combinational circuit designed to perform binary addition on multi-bit values. It is made up of cascading full adders, with each stage's carry output coupled to the following stage's carry input as represented in Fig. 2.

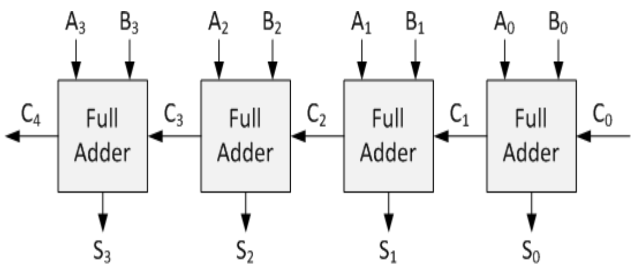

Fig. 2. Block Diagram of Ripple Carry Adder (RCA) [12], [19].

In a 4-bit Ripple Carry Adder, each complete adder adds the matching bits of the input operands to the carry from the previous stage. The carry propagates progressively from the least significant bit (LSB) to the most significant bit (MSB), thus the name "ripple carry adder" [12], [19].

B. LOGICAL AND

In an ALU, the AND operation is used for bitwise comparison and masking operations. It plays a significant role in control logic and data processing tasks. The logical AND operation is a basic digital operation that produces an

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output of ‘1’ only when all input bits are ‘1’. Otherwise, the output is ‘0’ [27].

C. LOGICAL OR

In ALU design, the OR operation is used in decision-making processes, bit setting operations, and combining multiple conditions. The logical OR operation produces an output of ‘1’ if at least one of the input bits is ‘1’. The output is ‘0’ only when all inputs are ‘0’ [26].

D. 4X1 MULTIPLEXER

A 4x1 multiplexer selects one of four input signals and routes it to a single output line based on the selected inputs. It functions as a data selector and is commonly employed in digital systems such as ALUs for operation selection. The 4x1 multiplexer consists of four data inputs D_0, D_1, D_2, D_3, two select lines S1 and S0, and one output Y. Depending on the combination of the select lines, one of the input signals is transmitted to the output [13].

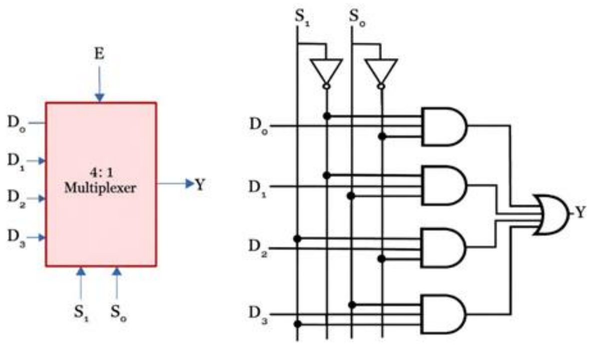

Fig. 4. Representation of conventional 4x1 Multiplexer [13].

TABLE II. TRUTH TABLE OF 4X1 MULTIPLEXER [13]

INPUTS		OUTPUT
S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

The Boolean expression for the output of a conventional 4x1 multiplexer:

$$Y = D_0S_1S_2 + D_1S_1S_0 + D_2S_1S_0 + D_3S_1S_0$$

A common 4x1 MUX employs fundamental logic gates like AND, OR, and NOT. Each input is coupled with the proper select line combinations using AND gates, and their outputs are then combined using an OR gate to form the final output.

Although these designs are functionally effective, they often suffer from certain limitations. One of the major drawbacks of conventional system is their excessive power consumption as a result of the enormous number of transistors. Additionally, increasing propagation delay and larger area constraints diminish the ALU’s overall efficiency. These limitations make traditional designs unsuitable for modern low-power, high-performance VLSI applications [20].

III. EXISTING SYSTEM-II

To address the constraints of standard CMOS-based ALU designs, a delay-controlled reconfigurable ALU has been presented in the literature by using reconfigurable logic structures to reduce hardware complexity and minimize latency, this design puts performance first. Important components of the delay-controlled reconfigurable ALU include a subtractor, AND and OR gates, an adder with a reconfigurable block, and a 4x1 multiplexer for operation selection. The main characteristic of the design is the reconfigurable block incorporated into the adder, which enables dynamic change of the critical route delay, hence enhancing both speed and efficiency [14].

A. HYBRID ADDER

The current design uses sophisticated structures like the Improved Adder (IA), Carry Input Selective Adder (CISA), and Carry Output Predicted Adder (COPA) to construct a hybrid reconfigurable adder. This design incorporates a reconfigurable block that dynamically modifies the delay during operation, in contrast to conventional ripple carry adders. Because the reconfigurable block is composed of CISA and COPA units, carry propagation is accelerated and latency is reduced.

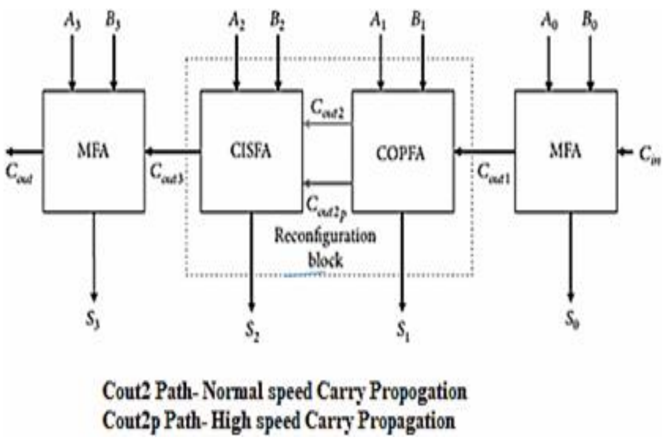

Fig. 4. Block representation of existing 4-bit Adder [15].

The IA block effectively generates sum and carry outputs by using multiplexing logic. By selecting suitable carry inputs, multiplexers help prevent unnecessary switching. While the COPA block predicts the carry output ahead of time, significantly reducing propagation latency, the CISA component enhances the carry selection process by applying logical criteria to pick the optimal carry path. In the reconfigurable adder, a CISA-COPA pair takes the place of the conventional IA + MUX21 combination. This hybrid method increases performance while lowering the crucial route delay brought on by carry propagation. Furthermore, the adoption of efficient logic architectures decreases

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transistor count, which results in lower power consumption and area [15].

1) INTERNAL STRUCTURE OF ADDER

The IA block is described as a modified full adder that uses two 2:1 multiplexer to generate the sum (S) and carry (Cout), with Cin as the selection input for the multiplexer. Its schematic in Fig. 6, uses an XOR gate, a NOT gate, and two MUX21 units. The XOR of A and B drives the select line of the first MUX and feeds the NOT gate, the MUXs choose between Cin and Cins to produce S and Cout. The IA aims to reduce transistor count and power compared to a conventional full adder.

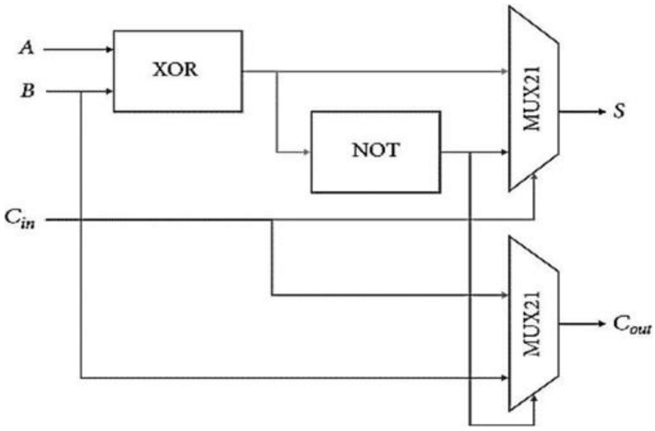

Fig. 5. Schematic of IA [15].

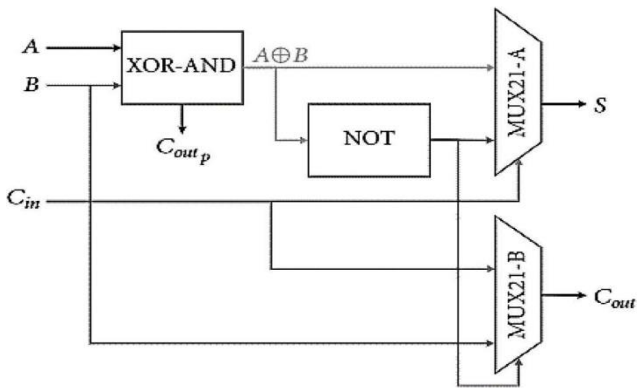

Fig. 6. Schematic of COPA [15].

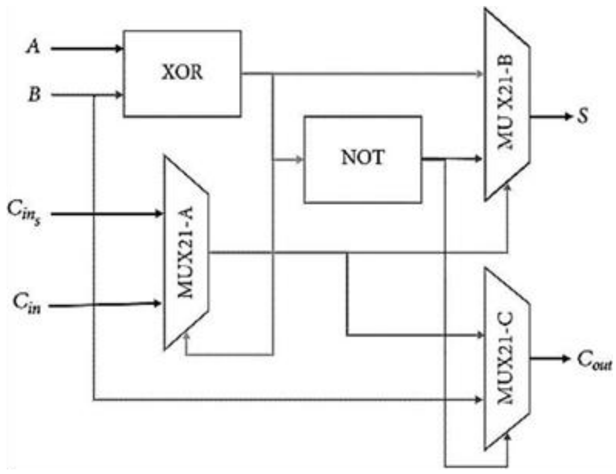

Fig. 7. Schematic of CISA [15].

CISA is a carry-input selecting adder. It uses the XOR of A and B to control a multiplexer that selects between two possible carry-in values (Cin and Cins). By selecting the appropriate carry-in based on AXORB, it shortens the carry propagation path and reduces delay. The schematic in Fig. 6, shows A and B feeding an XOR, whose output selects between Cin and Cins via MUX21-A, the selected carry feeds the other multiplexers for S and Cout.

COPA is a carry-output Predicted adder. It predicts both the actual carry output (Cout) and a predicted carry (Coutp). It includes an XOR-AND component (instead of a plain XOR) that generates the intermediate carry, when A and B are equal, this predicted carry is used, allowing faster data transmission to the CISA stage. Fig. 7, shows the COPA schematic with the XOR-AND gate producing the intermediate carry signal

B. SUBTRACTOR

A subtractor is a digital circuit that performs subtraction on two binary values. Subtraction is typically implemented in ALU architectures utilizing the idea of 2's complement. The subtraction operation A−B is performed as:

A−B = A + (2's complement of B)

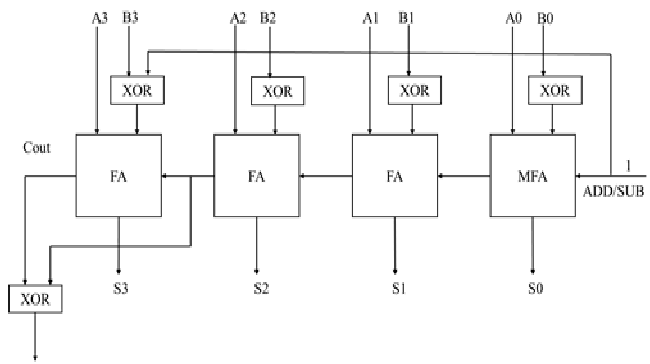

Fig. 8. Block Schematic representation of existing 4-bit Subtractor [17].

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This includes inverting all bits of B (1's complement), adding 1, and passing it into the circuit. The inversion of B is efficiently achieved using the XOR gates placed before each full adder stage. An XOR gate is used as a controlled inverter in the subtractor circuit as illustrated in Fig. 8. One input of the XOR gate is connected to the input bit of B, and the other input is connected to a control signal (mode signal) [16]. This control signal determines whether the circuit performs addition or subtraction.

- When control signal = 0 (Addition mode):
  $B \oplus 0 = B \rightarrow$ No change in input
- When control signal = 1 (Subtraction mode):
  $B \oplus 1 = B \rightarrow$ Input is inverted

Additionally, the control signal is also given as the initial carry input (Cin = 1) to complete the 2's complement operation [24].

C. AND GATE

The AND gate in the Fig. 9 is built with GDI (Gate Diffusion Input) based CNTFET logic, which decreases both transistor count and power consumption. In this design, the inputs are coupled so that the output is only active when both inputs are high. The usage of CNTFET results in reduced leakage current and enhanced performance [17].
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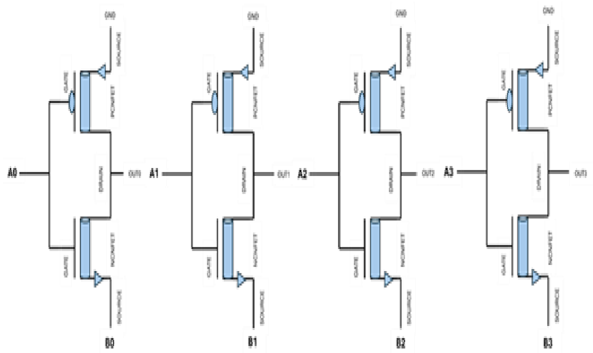

Fig. 9. Schematic representation of existing 4-bit AND gate [17].

TABLE III. TRUTH TABLE OF AND GATE [25], [26], [27]

INPUTS		OUTPUT
A	*B*	*Y*
0	0	0
0	1	0
1	0	0
1	1	1

D. OR GATE

The OR gate in the Fig. 10 is also built utilizing GDI logic and CNTFET technology. In this design, the inputs are applied to both p-type and n-type CNTFETs, resulting in an output derived by combining their drain terminals. The circuit is designed to produce complete voltage swing with little transistor consumption. When one of the inputs is high, the OR gate outputs a high value.

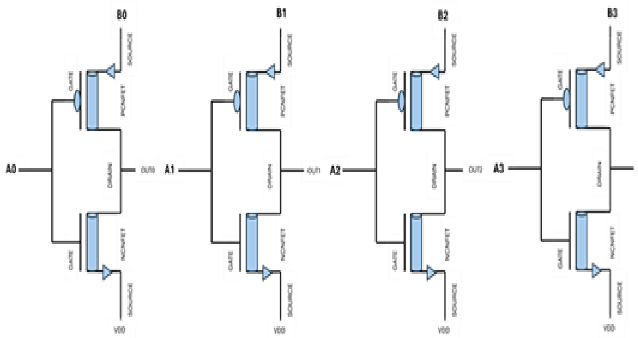

Fig. 10. Schematic representation of existing 4-bit OR gate [17].

TABLE IV. TRUTH TABLE OF OR GATE [26], [27]

INPUTS		OUTPUT
A	*B*	*Y*
0	0	0
0	1	1
1	0	1
1	1	1

E. HYBRID LOGIC 4X1 MULTIPLEXER

The 4x1 multiplexer is vital in the ALU since it selects the needed operation output. It employs hybrid logic and CNTFET-based 2x1 multiplexers. Initially, a 2x1 multiplexer is designed with GDI logic. To overcome voltage swing constraints, more CNTFET transistors are employed to achieve full output swing. A 4x1 multiplexer is made by joining several 2x1 multiplexers. Based on the select lines S1 and S0, the multiplexer selects one of four inputs [14].

3.1 CIRCUIT LEVEL IMPLEMENTATION

3.1.1 XOR

A fundamental component of the ALU, the XOR gate is especially used in arithmetic circuits such as adders and subtractors. To offer full voltage swing and improved performance, the XOR gate is constructed using CNTFET-based logic in the basic architecture. Only when the input signals change is the circuit supposed to provide a high output. The output remains low when both inputs are the same. Perfect rail-to-rail voltage swing is made possible by the recommended XOR configuration in Fig. 11, which enhances signal integrity and reduces static energy degradation [18].

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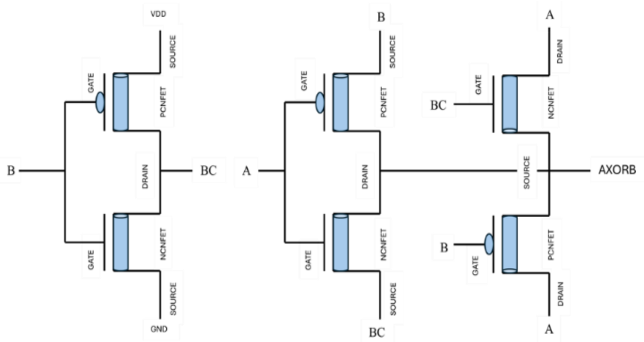


Fig. 11. Transistor level of CNTFET-based XOR gate [18].

Additionally, compared to conventional CMOS implementations, the XOR gate is enhanced by hybrid logic techniques that help lower the number of transistors. Increasing the ALU's arithmetic operations' efficiency depends on this simplified design.

3.1.2. 2X1 MULTIPLEXER

To reduce power consumption and transistor use, the 2x1 multiplexer makes use of CNTFET technology with GDI logic. This design's basic multiplexer structure consists of two CNTFET transistors. However, in Fig. 12, an additional transistor is introduced in order to ensure complete swing output due to the restricted voltage swing in GDI logic.

The select line controls the output selection:

- When the select input is '0', input I_0 is passed to the output
- When the select input is '1', input I_1 is passed to the output

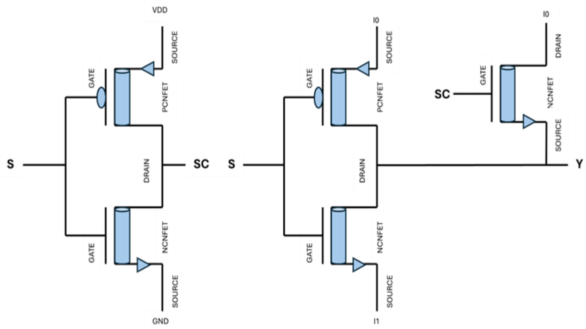


Fig. 12. CNTFET based existing 2x1 MUX [18].

This streamlined approach preserves high-speed operation while lowering hardware complexity.

3.1.3 4X1 MULTIPLEXER

Several refined 2x1 multiplexers are combined to create the 4x1 multiplexer shown in Fig. 13. It consists of four input lines, two select lines, and one output. Based on the select inputs S_1 and S_0, one of the four inputs is transmitted to the output. The implementation uses hybrid logic with CNTFET devices.

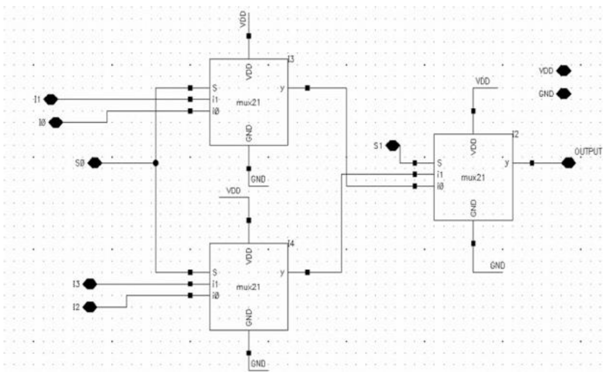


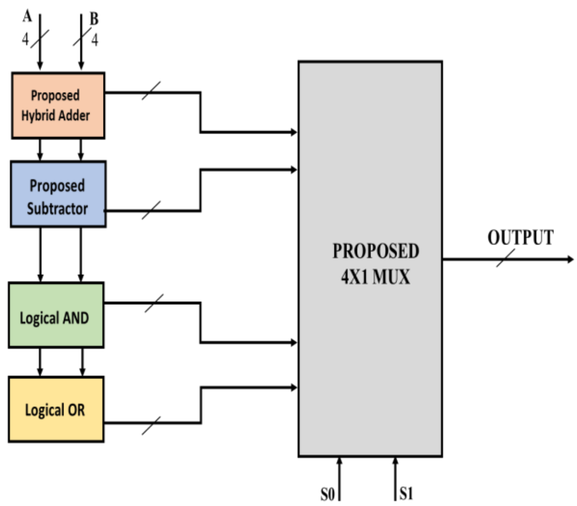
Fig. 13. CNTFET based existing 4x1 MUX [18].

Thus, the integration of hybrid logic-based adder, efficient subtractor, optimized logic gates, a reconfigurable multiplexer and the circuit level implementation of XOR, 2x1 multiplexer, and 4x1 multiplexer using CNTFET and hybrid logic techniques enables the ALU to achieve high performance with reduced power, delay, and hardware complexity [18].

IV. PROPOSED SYSTEM

To further enhance the performance of the delay-controlled reconfigurable ALU, an optimized design is proposed by reducing the transistor count at the module level while maintaining the overall architecture of the existing system.

The proposed ALU has the same basic structure as the existing delay-controlled reconfigurable ALU, with arithmetic modules (hybrid adder and subtractor), logical units (AND and OR gates), and a 4x1 multiplexer for operation selection as represented in Fig. 14. However, changing the underlying submodules employed within these blocks results in considerable improvements. This study optimizes critical components, including the XOR gate, 2x1 multiplexer, and 4x1 multiplexer, to minimize transistor count. Because these parts are widely employed in the development of adders, subtractors, and selection circuits, optimizing them reduces total hardware.



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Vol 26 Issue 04(April),2026
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Fig. 14. Block representation of proposed delay controlled reconfigurable ALU.

A. *Circuit Level Implementation*

1. *XOR*

The optimized XOR gate in Fig.15, is utilized in adder and subtractor circuits, most notably for sum generation and conditional inversion in two's complement operations. In the proposed design, the XOR gate is implemented using an optimized transistor-level structure to lower the number of transistors in the XOR architecture. The circuit is designed such that the output is high only when the inputs are different and low when the inputs are same. Compared to the conventional and existing XOR implementations, the proposed design minimizes the number of transistors by using an efficient arrangement of pull-up and pull-down networks. This design ensures proper logic functionality while reducing switching activity and internal capacitance, which directly contributes to lower power consumption. Additionally, the reduced number of transistors improves propagation delay, resulting in faster operation.

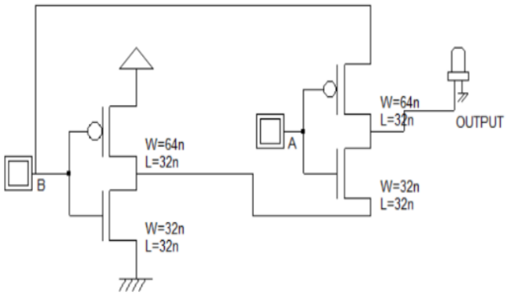

Fig. 15. Schematic representation of Proposed XOR gate.

2. *2X1 MUX*

The 2x1 multiplexer is designed using an optimized transistor configuration to reduce hardware complexity. It consists of two inputs A and B, one select line (S), and one output (Y) as in the Fig. 16.

The operation of the circuit is as follows:

- When S = 0, output Y = A
- When S = 1, output Y = B

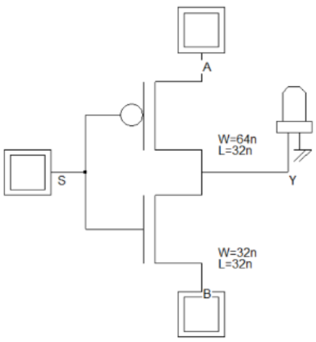

Fig. 16. Schematic representation of Proposed 2x1 MUX.

In the proposed design, the multiplexer is implemented using a minimal number of transistors compared to conventional CMOS or GDI-based designs. The circuit efficiently passes the selected input to the output with reduced voltage degradation. By minimizing the transistor usage, the proposed 2x1 multiplexer achieves reduced power consumption, lower propagation delay and improved area efficiency. This optimized multiplexer is further used as a building block for constructing higher order multiplexers such as the 4x1 mux.

3. *4X1 MUX*

The 4x1 multiplexer in the proposed system in Fig. 17, is constructed using improved 2x1 multiplexers, thereby inheriting the advantages of reduced transistor count and improved efficiency. It consists of four inputs, two select lines (S_1 and S_0) and one output (Y). Based on the select inputs, one of the four inputs is selected and transmitted to the output.

The proposed design reduces the number of the multiplexing stages and transistor usage by efficiently combining lower-level multiplexers. This leads to improved signal propagation and reduced delay. Since the 4x1 MUX is used in the ALU for selecting arithmetic and logical operation outputs, its optimization significantly enhances overall system performance.

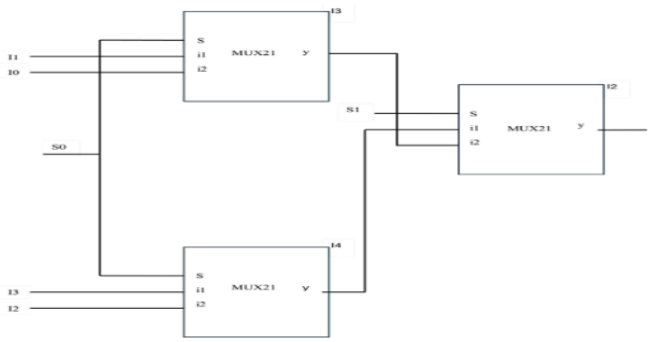

Fig. 17. Schematic representation of Proposed 4x1 MUX.

Although the ALU's functional design stays unaltered, the proposed circuit improvements improve performance metrics. It focuses on circuit-level optimization by redesigning fundamental sub-modules such as the XOR gate, 2x1 multiplexer, and 4x1 multiplexer. These optimizations result in the reduction of transistor count which instantly results in lower power consumption, shorter propagation delay and higher area efficiency. Thus, the proposed system achieves better efficiency and high performance compared to the existing delay-controlled reconfigurable ALU, making it more suitable for low-power VLSI applications.

B. *Area Evaluation Methodology*

The area evaluation methodology compares the existing systems with the proposed system by quantifying both the number of basic logic blocks and the total transistor count required for each design. Area is a crucial parameter in the construction of digital circuits because fewer blocks and

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transistors usually result in smaller silicon areas, low power consumption and increased efficiency.

TABLE V. BLOCK COUNT OF EXISTING AND PROPOSED SYSTEMS

	XOR	2-INPUT AND	2-INPUT OR	4-INPUT MUX	2-INPUT MUX	TOTAL
Existing System-1	20	19	11	1	--	51
Existing System-2	16	11	6	1	21	55
Proposed System	16	11	6	1	21	55

TABLE V represents the Block Count, shows how many of each fundamental component are used in each system. The Existing System-1uses 51 blocks and the Proposed System uses 43 blocks, matching Existing System-2, which means the structural composition of blocks is the same for these two

TABLE VI represents the Transistor Count which converts the block count into actual transistor numbers by multiplying the count of each block by the number of transistors needed to implement it. The total count shows the number of transistors used in each system.

As a whole, the Proposed System decreases the overall transistor count from 292T to 214T, or around 27%, while achieving the same block count as Existing System-2. More effective implementations of the XOR (4T vs 6T), the 4-input MUX (6T versus 15t), and the 2-input MUX (2T versus 5T) are mostly responsible for this reduction. The outcome shows that the suggested design maintains the same logical structure while being more space-efficient.

TABLE VI. TRANSISTOR COUNT OF EXISTING AND PROPOSED SYSTEM

	XOR	2-INPUT AND	2-INPUT OR	4-INPUT MUX	2-INPUT MUX	TOTAL
Existing System-1	20X12T=240	19X6T=114	11X6T=66	1X94T=94	--	514T
Existing System-2	16X6T=96	11X8T=88	6X8T=48	1X15T=15	21X5T=105	352T
Proposed System	16X4T=64	11X8T=88	6X8T=48	1X6T=6	21X2T=42	248T

V. RESULTS AND DISCUSSION

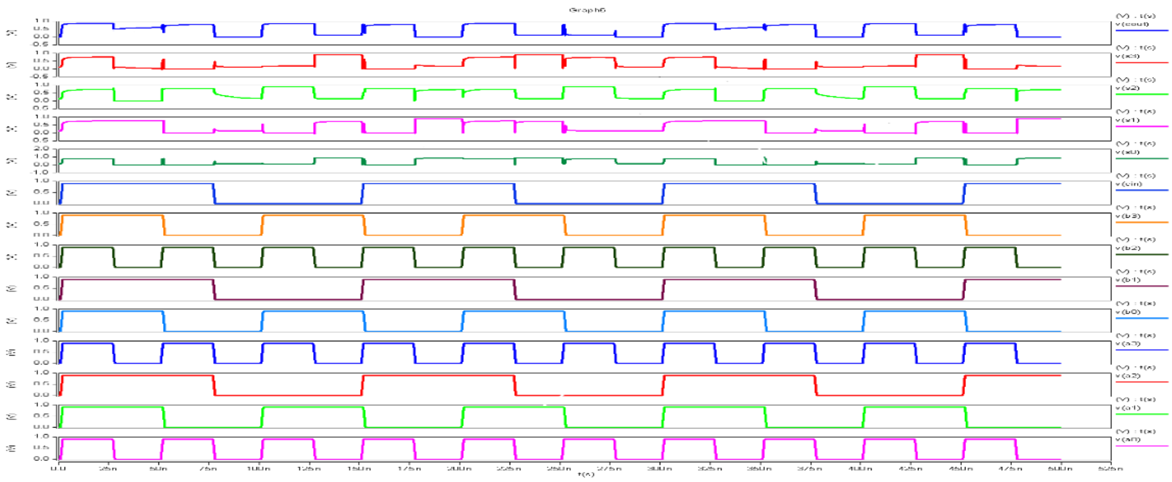

Fig. 18. Transient simulation of the Proposed CNTFET based Hybrid 4-bit Adder

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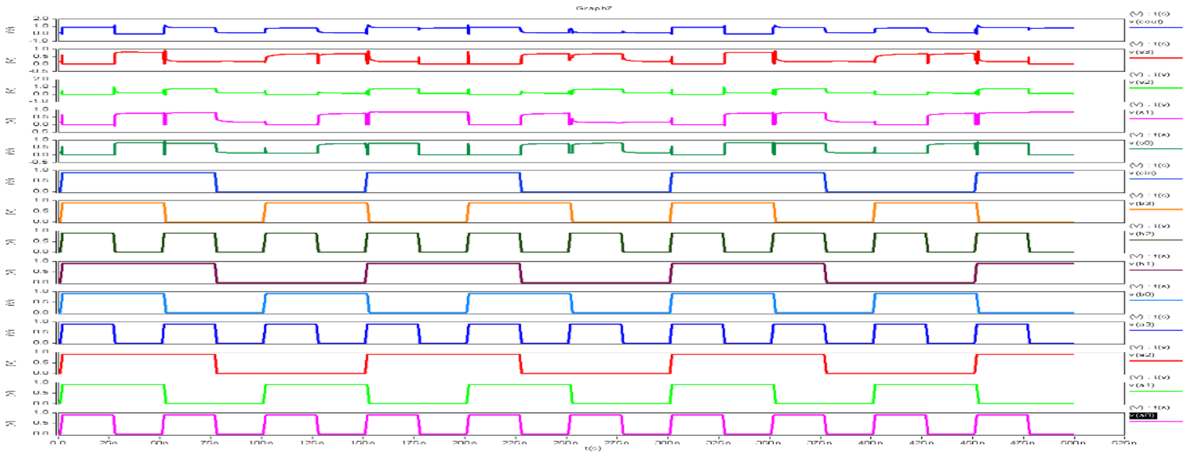

Fig. 19. Transient simulation of the Proposed CNTFET based 4-bit Subtractor

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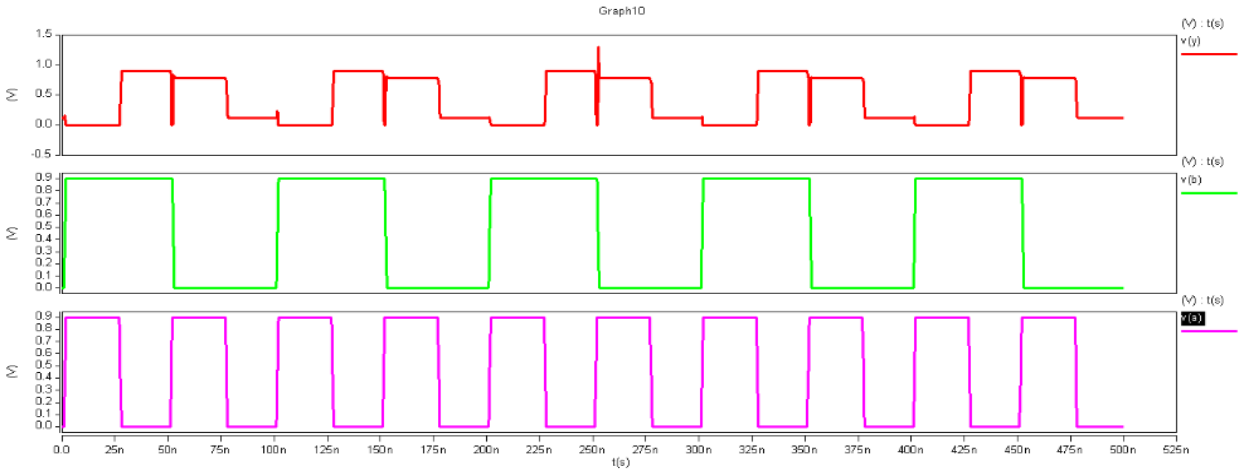

Fig. 20. Transient simulation of the Proposed CNTFET based rail-to-rail swing XOR gate.

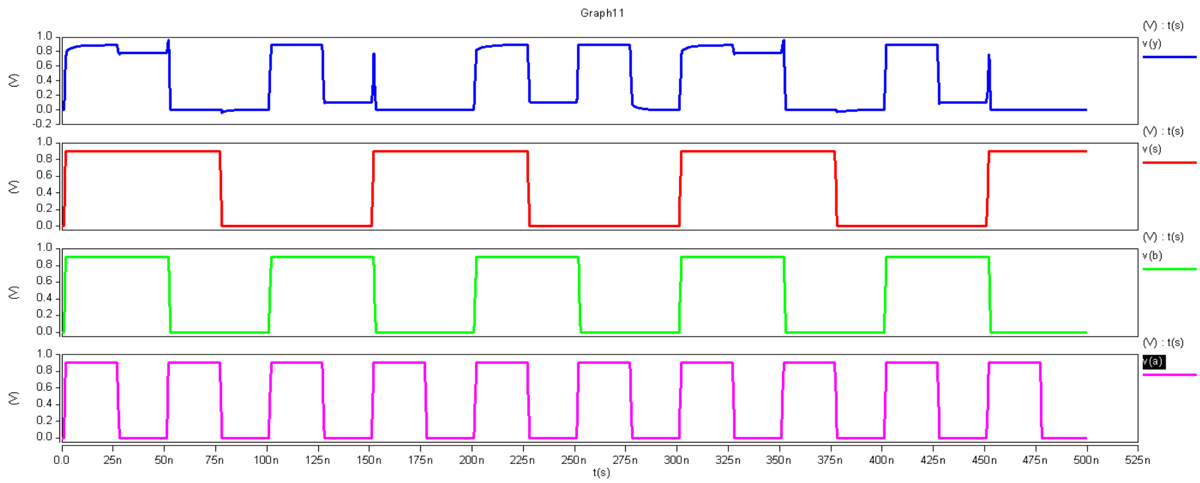

Fig. 21. Transient simulation of the Proposed CNTFET based full swing 2x1 MUX.

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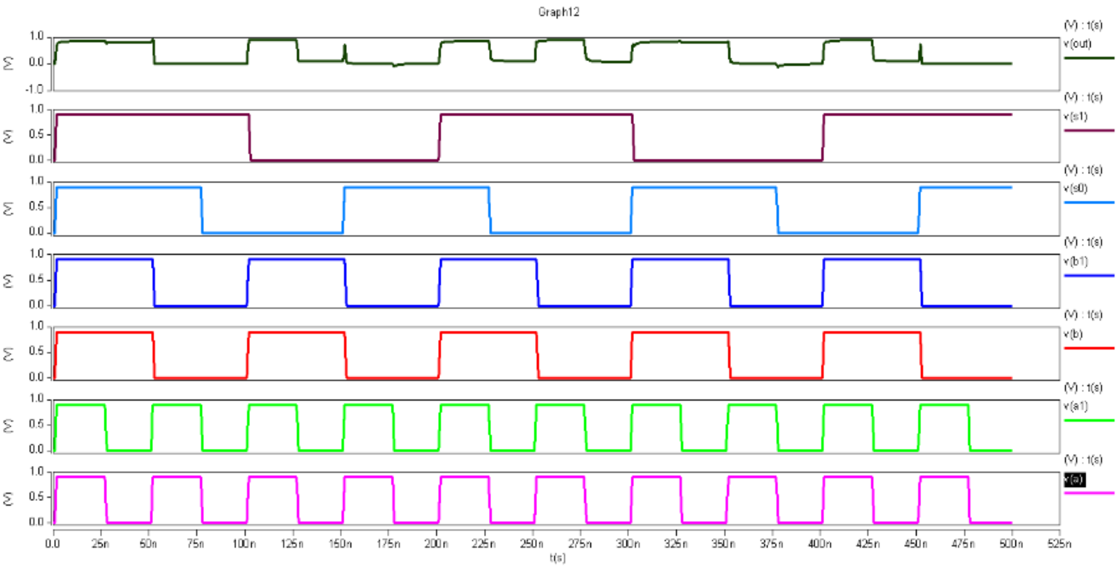

Fig. 22. Transient simulation of the Proposed CNTFET based rail-to-rail swing 4x1 MUX.

In Fig. 18, the suggested CNTFET-based hybrid 4-bit adder's transient simulation results are displayed. The resultant sum bits S [3:0] and carry output (Cout) are noticed after applying the input signals A [3:0] and B [3:0] together with the carry input (Cin). With complete rail-to-rail voltage swing and abrupt transitions, the waveform shows accurate arithmetic addition for all input combinations. The carry output shows the correct carry propagation across each step, and the adder generates the sum output as $S = A \oplus B \oplus Cin$. The simulation verifies that the suggested hybrid adder functions well with low latency and steady output levels.

The transient simulation of the suggested CNTFET-based 4-bit subtractor is shown in Fig. 19. Using 2's complement arithmetic, the subtraction A-B is carried out by applying an initial carry input Cin = 1and inverting the subtrahend B using XOR gates that are controlled by a mode signal. The waveform displays the mode control signal, the input operands A [3:0] and B [3:0], and the difference D [3:0] with the borrow output. The XOR gates invert B when the mode signal is 1, and the adder executes A + (~B) + 1 to provide the right difference. The simulation confirms precise subtraction with minimal glitches and complete voltage swing.

Fig. 20, shows the transient simulation of the suggested CNTFET-based XOR gate. The output Y is monitored as the inputs A and B are changed in every conceivable combination (00, 01, 10, 11). According to the logic $Y = A \oplus B$, the waveform demonstrates that the output Y only rises when A and B are different and stays low when they are the same. The output displays a complete rail-to-rail swing, demonstrating that the improved transistor configuration delivers smooth, quick transitions and removes voltage degradation.

Fig. 21, shows the suggested transient simulation of the CNTFET-based 2x1 multiplexer. The output Y is tracked while the inputs A and B are applied in conjunction with the select line S. The output Y comes after input A when S = 0 and input B when S = 1. The waveform, which reflects the fewer transistors and enhanced driving capabilities of the suggested design, validates the proper choice of the input signal with full swing at the output and a very short propagation delay.

The transient simulation of the suggested CNTFET-based 4x1 multiplexer is displayed in Fig. 22. After applying the two select lines S1 and S0 as well as the four data inputs I0, I1, I2, and I3, the output Y is noted. The output corresponds to the relevant input based on the select line combination: Y=I0, when S1S0=00, Y=I1 when S1S0=01, Y=I2 when S1S0=10, and Y=I3 when S1S0=11. The waveform highlights the effectiveness of the suggested multiplexer constructed from optimized 2x1 MUX stages by displaying precise data selection with complete rail-to-rail swing and minimal latency.

TABLE VII. PERFORMANCE ANALYSIS OF PROPOSED ALU

	Power Consumption	**Delay(ns)**	**PDP($x10^{-18}$) in J**	**EDP($x10^{-27}$) in Js**
4-bit Proposed Adder	1.47	0.00139	2.04	0.00284

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4-bit Proposed Subtractor	1.43	0.109	156	17.0
Proposed 4X1 MUX	0.000381	0.226	86.1	19.5
Proposed 4-bit ALU	0.977	0.956	934	893

TABLE VII shows the Performance Analysis of Proposed ALU which summarizes the key efficiency metrics of the proposed 4-bit ALU and its individual modules (adder, subtractor, 4x1 MUX). It reports the four parameters: power Consumption, Delay, PDP and EDP. Power Consumption indicates the average power drawn by each module during operation. The low values of the modules reflect the benefit of using CNTFET technology and optimized transistor-level designs, which reduce leakage and switching power. The propagation delay is represented from input change to stable output. The very low delay and PDP of the adder shows its suitability for high-speed, low-energy and effectiveness of the hybrid logic implementation. EDP emphasizes both energy efficiency and speed, confirming that the proposed design achieves a good trade-off between speed and power.

Table VIII, presents a comparative performance analysis of different previously reported designs with proposed 4-bit LU, focusing on key metrics such as power consumption, delay, Power Delay Product (PDP), and Energy Delay Product (EDP). It is evident from the statistics that the suggested 4-bit ALU performs better than all current solutions in every way. With the lowest power usage of 7.77nW, it demonstrates exceptional energy efficiency. In a similar vein, the latency is drastically decreased to 12.87 ns, indicating faster processing performance in comparison to previous efforts. The suggested design records the lowest value of 99.99 × 10^{-11} J, indicating its optimal balance between low power and good performance, as PDP is a measure of the trade-off between power and speed. Additionally, compared to the other references, the EDP, which represents overall energy efficiency including delay impact, is significantly reduced to 1286.8 × 10^{-22} Js. Overall, the findings demonstrate how effective the suggested ALU architecture is, providing significant gains in speed, power usage and energy-efficiency.

TABLE VIII. COMPARISON OF POWER AND ENERGY EFFICIENCY IN 4-BIT ALU DESIGNS

	[28]	**[29]**	**[30]**	**[8]**	**[18]**	**Proposed 4bit ALU**
Power Consumption (nW)	24.6	15.6	14.6	17.2	11.1	7.77
Delay (nS)	117.2	96.83	87.3	88.2	42.9	12.87
PDP ($x10^{-18}$) in J	2883.2	1501.5	1274.5	1517.4	476.1	99.99
EDP ($x10^{-27}$) in Js	337911.4	145390.2	111263.8	133834.6	20424.6	1286.8

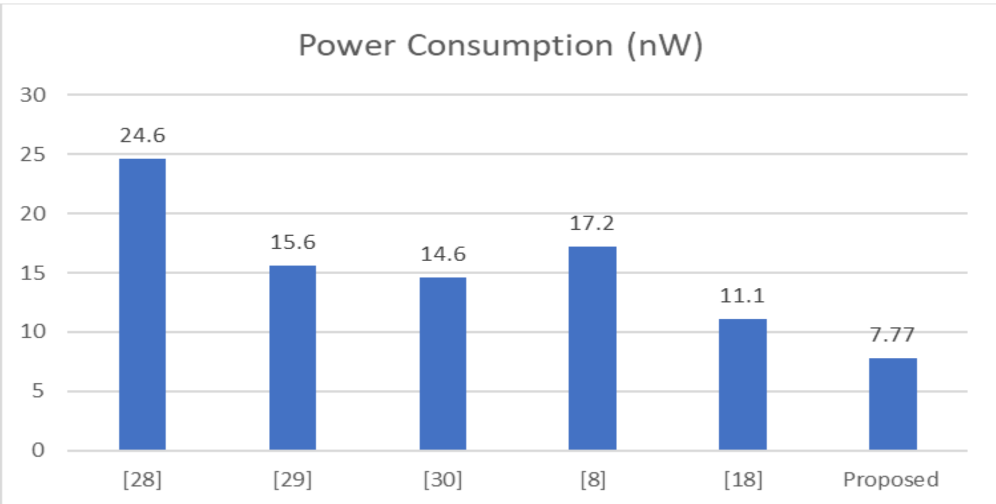

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Fig. 23. Comparison of Power Consumption for Various 4-Bit ALU Designs.

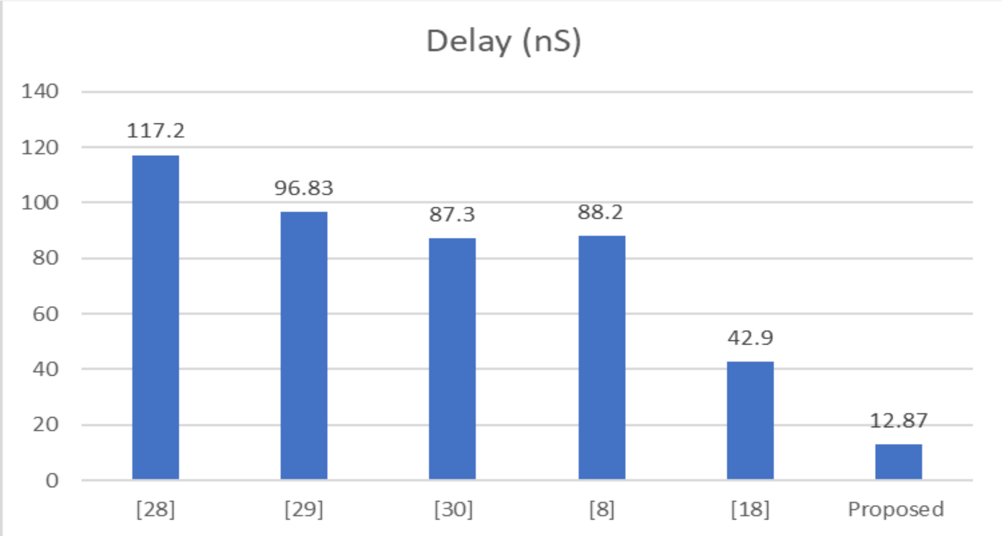

Fig. 24. Comparison of Propagation Delay for Various 4-Bit ALU Designs.

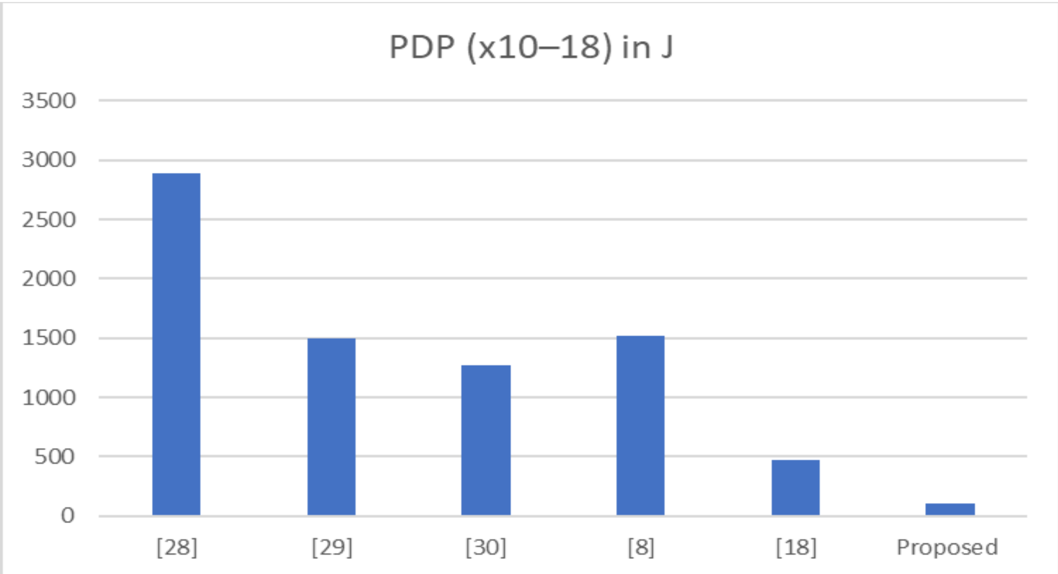

Fig. 25. Comparison of Power Delay Product (PDP) of 4-Bit ALU Designs.

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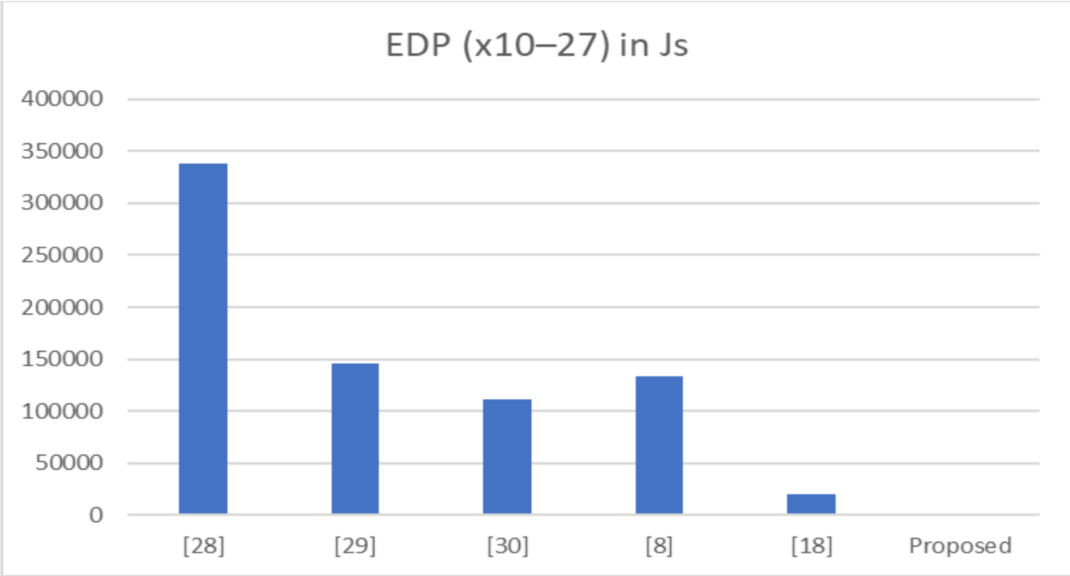

Fig. 26. Comparison of Energy Delay Product (EDP) of 4-Bit ALU Designs.

The power consumption of several 4-bit ALU architectures is depicted in Fig. 23. The suggested ALU's higher energy efficiency is demonstrated by the fact that it uses the least amount of power out of all the designs that were examined. The suggested design is more suited for low-power VLSI applications because to the power savings.

The delay performance of several ALU architectures is contrasted in the Fig. 24. With the least amount of delay, the suggested 4-bit ALU operates more quickly. It is hence very effective for high-performance computing applications.

The PDP values, which show the trade-off between speed and power usage, are shown in the Fig. 25. The suggested ALU has the lowest PDP, demonstrating the best possible compromise between high performance and low power.

The EDP comparison, which assesses overall energy efficiency while taking delay into account, is depicted in the Fig. 26. The Suggested architecture is extremely efficient in terms of both energy usage and computing speed since it achieves the minimal EDP.

Power consumption, delay, and power-delay product (PDP) for the suggested 4-bit ALU and the existing designs are compared in the Fig. 27. The efficiency advantages of the suggested design may be evaluated immediately since the bar chart displays the three important performance criteria side by side. Because of the use of low-leakage CNTFET transistors, improved transistor size, and decreased switching activity in the arithmetic blocks, the proposed 4-bit ALU uses an order of magnitude less than the reported designs because of a simplified critical route, lower node capacitance, and quicker carry generation. Additionally, it achieves a propagation latency as opposed to the compared designs, respectively. This is because the signal transitions across the 4-bit word more quickly because to a simplified critical path, lower node capacitance, and faster carry generation. The proposed ALU records a PDP which is significantly lower than the observed referenced works. This indicates that the proposed ALU not only saves energy-delay trade-off but also operates quickly by reducing the power. In general, the findings shown in Fig. 22. Show that the suggested 4-bit ALU performs better than the current designs in all the three criteria, making it the fastest and the most energy-efficient of the five.

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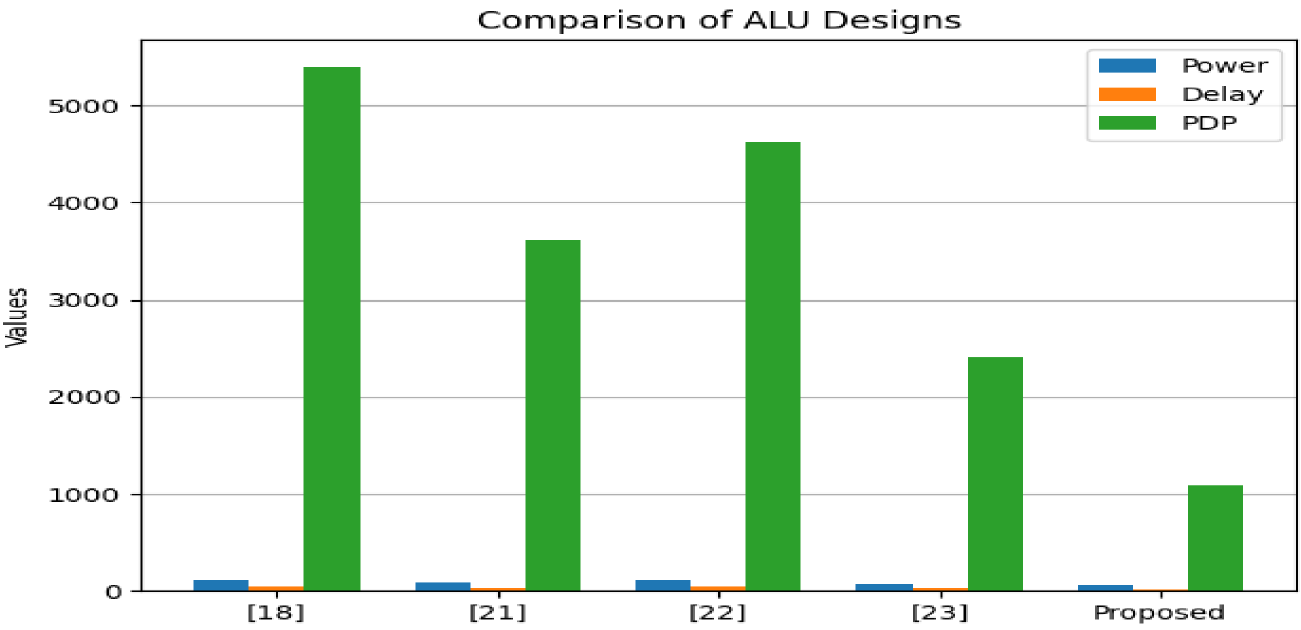

Fig. 27. Variation of Performance Parameters of the Proposed Reconfigurable 4-bit ALU compared to Existing Architectures.

VI. Conclusion

This work successfully presents a low-power, delay-controlled 4-bit ALU design using CNTFET technology, focusing on transistor-level optimization of critical submodules. By redesigning key components such as XOR gate, 2x1 multiplexer, and 4x1 multiplexer, the proposed system significantly reduces transistor count while maintaining the overall architecture of the existing delay-controlled ALU. The Proposed design achieves a 27% reduction in transistor count, which directly contributes to lower power consumption, reduced propagation delay, and improved area efficiency. Simulation result obtained using HSPICE validate that the ALU operates with full voltage swing, minimal glitches, and faster switching characteristics. PDP and EDP have significantly improved, according to the performance study, demonstrating an effective trade-off between speed and energy usage. The suggested ALU performs better in terms of speed and power efficiency when compared to traditional CMOS-based and current CNTFET-based systems. These enhancements make it ideal for contemporary VLSI applications, including as embedded systems, portable electronics, and Internet of Things devices, where low power improves scalability and resilience.

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