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Design And Implementation of 2D FIR Filter using modified adder and multiplier

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***Abstract*— This project focuses on the design and implementation of a two-dimensional (2D) Finite Impulse Response (FIR) filter using Verilog, targeting a Spartan-6 FPGA for real-time image processing applications. The objective is to enhance computational efficiency and optimize hardware utilization by addressing limitations found in conventional FIR filter architectures, such as high propagation delays caused by ripple carry adders (RCA). To improve performance, the proposed system replaces the RCA with a compressor adder and evaluates two architectural variations—one using sequential processing without data broadcasting and another employing parallel processing with data broadcasting. The design is synthesized and simulated using Xilinx Vivado and evaluated across multiple configurations (3-tap, 6-tap, and 12-tap). Experimental results demonstrate that the data broadcast architecture, in conjunction with the compressor adder, significantly improves processing speed and reduces power consumption without increasing logic utilization. The proposed system presents a scalable and efficient solution suitable for high-performance digital filtering applications in real-time environments.**

Keywords: Filter, broad cast, adder, multiplier

1. Introduction

Finite Impulse Response (FIR) filters are a fundamental component of digital signal processing systems, valued for their stability, linear phase characteristics, and ease of implementation. FIR filters respond only to a finite number of input samples, which simplifies the design and avoids issues of feedback and instability commonly found in Infinite Impulse Response (IIR) filters. These attributes make FIR filters highly suitable for applications such as image processing, audio enhancement, and biomedical signal conditioning.

Traditional FIR Filter Design

A basic FIR filter is implemented using a series of multiplication and accumulation operations, mathematically described by the convolution of input signals with filter coefficients. The standard 1D FIR filter equation is given by:

$$y(n) = \sum_{k=0}^{N-1} h(k).x(n-1)$$

Where:

y(n) is the output signal,

x(n) is the input signal,

h(k) are the filter coefficients (also known as taps),

N is the number of taps (filter length).

In 2D FIR filters, which are used in image processing, the convolution operation extends over both horizontal and vertical dimensions. The 2D FIR output is calculated as:

$$y(m,n) = \sum_{i=0}^{M-1} \sum_{j=0}^{N-1} h(i,j).x(m-i, n-j)$$

Where h(i,j) is the 2D filter kernel and x(m,n) is the input image.

Use of Multipliers and Adders

The core of FIR filter implementation lies in the repeated use of multipliers and adders. Each input sample must be multiplied by a corresponding coefficient, and the results must be summed to generate the output. This operation is resource-intensive, particularly when implemented on hardware such as Field Programmable Gate Arrays (FPGAs), where logic elements and memory blocks are limited.

To address hardware complexity, various multiplier optimization techniques have been proposed:

1. Booth Multipliers
2. Wallace Tree Multipliers
3. Distributed Arithmetic (DA)
4. Canonical Signed Digit (CSD) Representation

Despite these methods, multiplication remains one of the most resource-demanding operations in FIR filter design.

1. Filter Coefficient Optimization

The performance of an FIR filter is significantly influenced by its coefficients, which determine the filter's frequency response. Coefficient values are often derived using mathematical tools like the Window Method, Frequency Sampling Method, or Parks–McClellan Algorithm. In practical scenarios, tools like

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MATLAB's Filter Design and Analysis (FDA) Tool are used to generate coefficients based on user-defined specifications such as cut-off frequency, passband ripple, and stopband attenuation.

Challenges:

Quantization Errors: Coefficients must be represented in fixed-point format, introducing rounding errors.
Symmetry Constraints: To reduce computational effort, symmetric filters are often used, which limits flexibility in frequency response shaping.
Trade-offs: A balance must be struck between filter performance (sharpness, transition width) and implementation cost (number of taps, bit width).
Summary of Traditional Architectures

Traditional FIR architectures follow a direct-form structure, where delay elements, multipliers, and adders are organized linearly. While effective, this design approach can become inefficient in terms of area, speed, and power when scaled to higher dimensions or tap lengths. As a result, modern FIR implementations seek optimization through architectural innovations such as:
1. Pipelining to increase throughput.
2. Parallel Processing to reduce latency.
3. Compressor Adders to minimize delay in summation paths.
4. Data Broadcasting to improve input access speed in 2D filtering.

2.Related Work
Numerous research efforts have been directed toward improving the efficiency, speed, and power consumption of 2D FIR filters for real-time digital signal processing applications. Odugu [1] proposed a VLSI architecture using high-speed, low-power multipliers along with Carry Look-Ahead (CLA) adders, which improved area and delay performance but introduced complexity in larger designs. Gade and Uppala [2] introduced higher-order symmetric FIR filters using Canonical Signed Digit (CSD) representation and Common Subexpression Elimination (CSE), which made coefficient optimization more efficient, though at the cost of increased design effort.
Reddy and Juliet [3] utilized Circular Symmetry and Common Subexpression Overlap-Avoidance (CSOA) to reduce redundant computations and hardware resources, but their design encountered quantization issues. Similarly, Merfeena [4] adopted approximate multipliers for low-power filtering, which effectively reduced critical path delay, but at the expense of computational accuracy, making it unsuitable for precision-critical tasks. Matei and Chiper [5] explored a polyphase differentiator architecture for 2D FIR filters that achieved low latency and dynamic power reduction, although the analytical design process was complex and less flexible.
For biomedical signal processing, Kumar and Chinnapurapu [6] developed a filter using a Radix-2r multiplier, targeting low power and optimized logic for electrooculography (EOG) signal denoising. Despite its efficiency, the design faced integration challenges in general-purpose image processing. Vijetha and Naik [7] used Distributed Arithmetic (DA) in block FIR filters to achieve high-speed parallelism, which was beneficial in terms of speed, but resulted in power and area trade-offs in higher-order filters. Chowdari and Beatrice [8] improved this design using multiplexer logic to reduce path delay, but their method led to memory overhead and a loss in dynamic range.
Kishore Kumar [9] proposed a hybrid FIR filter combining radix-2r multiplication and memory optimization to reduce switching activity and noise. However, it faced bottlenecks when processing high-resolution image data. Mamidala and Qureshi [10] leveraged Wallace Tree Adders and CSD-based coefficient generation for high-speed phase-based FIR filtering, but the design complexity and quantization errors limited its practical usability. A novel use of
diagonal and quadrantal symmetry in 2D FIR filters was presented by Reddy and Juliet [11], which enhanced area efficiency but was restricted to specific symmetric kernels.
Earlier foundational works, including Azimi-Sadjadi and Rostampour [12], proposed parallel and pipelined 2D FIR processing architectures that influenced many modern designs, though they are outdated in terms of current FPGA optimization capabilities. The textbook by Proakis and Manolakis [13] serves as a theoretical cornerstone for FIR filter design but lacks focus on implementation in modern hardware environments. More recent studies, such as those by Johnson and Smith [14], explored FPGA-specific implementations with pipelining and symmetry for speed optimization, and Lee and Kim [15] emphasized power-efficient architectures, though both faced trade-offs in logic complexity and resource usage.
Overall, the literature reveals a strong focus on enhancing filter speed and reducing area and power consumption. However, recurring challenges—such as propagation delays from ripple carry adders, limitations in coefficient handling, and inefficiencies in data flow—persist. These limitations motivate the current

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project, which proposes the use of compressor adders and data broadcasting techniques to improve processing speed, reduce power, and maintain scalability for real-time FPGA-based 2D FIR filter implementations.

2. Proposed work

An optimized two-dimensional (2D) finite impulse response (FIR) filter architecture is proposed to enhance hardware resource utilization, reduce propagation delay, and improve overall computational efficiency. In contrast to conventional designs that employ ripple-carry adders (RCAs), the proposed architecture replaces RCAs with compressor adders, significantly reducing the critical path delay and thereby increasing processing speed. Furthermore, the window coefficient values are optimized to w1=[0.5, 1.0, 0.5]w_1 = [0.5,\ 1.0,\ 0.5]w1=[0.5, 1.0, 0.5] and w2=[0.3, 0.6, 0.3]w_2 = [0.3,\ 0.6,\ 0.3]w2=[0.3, 0.6, 0.3], resulting in improved frequency response and enhanced filter performance. The proposed design is developed, synthesized, and verified using Xilinx Vivado and implemented on a Spartan-6 FPGA, demonstrating efficient and reliable hardware realization.

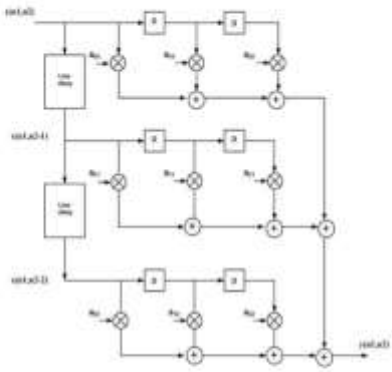

Fig.1 Proposed 2D FIR filter without broad cast using modified adder

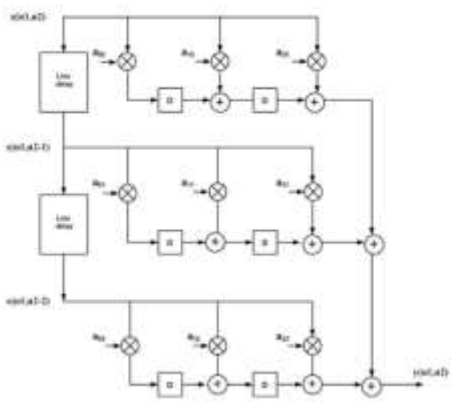

Fig.2 Proposed 2D FIR filter with broad cast using modified adder

3. Results and Analysis

The proposed 2D FIR filter was implemented on a Spartan-6 FPGA and evaluated using Xilinx Vivado for 3-tap, 6-tap, and 12-tap configurations. The findings demonstrate significant improvements in processing speed, power efficiency, and area utilization.

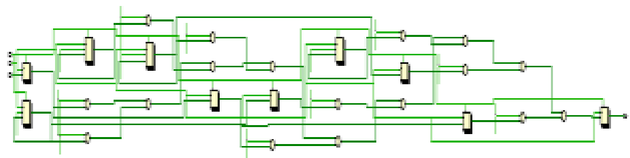

Fig. 3 RTL schematic of 2D FIR filter without data broadcast structure

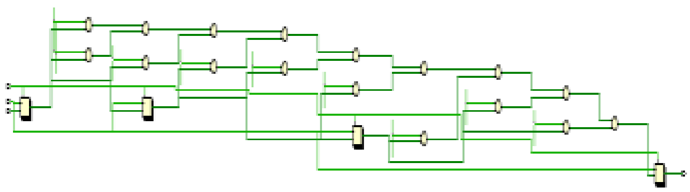

Fig. 4. RTL schematic of 2D FIR filter with data broadcast structure

Fig. 5. Simulated waveform for 2D FIR filter

Table 1. Synthesis results for implemented 2D FIR filter

Proposed Structures	Area (LUT)	Speed (ns)	Power (Watt)
2D data broadcast FIR digital filter design	37LUT (0.19%)	6.9655	0.1619 W
2D non-broadcast FIR digital filter design	37 LUT (0.19%)	6.8352	0.1813 W

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1. Conclusion

In One of the main optimizations made to the suggested system was the substitution of a compressor adder for the ripple carry adder (RCA), which greatly decreased propagation delay and increased computational efficiency. The FIR filter's scalability and efficacy across varying levels of complexity were demonstrated by its implementation in 3-tap, 6-tap, and 12-tap configurations. In comparison to traditional FIR filter designs, the suggested architecture delivers lower power consumption, reduced space utilization, and higher processing speed, as confirmed by the simulation and synthesis results.

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