Design of the Adaptive LMS Filter For ECG Signal Noise Reduction

K Chandana Priya [1], N Swathi [2], T G Tejaswini[3]

[1]*PG Scholar,* [2]*Assistant Professor,*[3]*Assistant Professor, Dept of ECE, Anantha Lakshmi institute of technology & sciences, Anantapuramu.*

ABSTRACT

In this project, we aim to explore and address the core challenges associated with the chosen subject. By investigating both theoretical and practical aspects, the paper intends to present a comprehensive analysis that contributes to existing knowledge. The research methodology encompasses various data collection techniques, including surveys, interviews, and case studies, ensuring the acquisition of diverse perspectives. Through this multifaceted approach, the paper seeks to uncover key insights that can inform future strategies and solutions. Furthermore, the project emphasizes the importance of collaborative efforts, drawing on interdisciplinary resources to enhance the quality and applicability of the findings. Ultimately, this work aspires to offer valuable recommendations and innovative solutions that can be utilized in real-world scenarios, benefiting both practitioners and researchers alike. By bridging the gap between theory and practice, the project aims to make a meaningful impact in the field.

Keywords: Challenges,Theoretical,Practical,Analysis,Methodology,Datacollection, Perspectives, Collaborative, Recommendations, Innovative

I. INTRODUCTION

The electrocardiogram (ECG) is a crucial diagnostic tool in cardiology, but its effectiveness can be hindered by various noise sources, including baseline drift, power line interference, and muscle artifacts. To improve ECG signal quality, adaptive filtering techniques such as the Least Mean Square (LMS) filter are commonly used. These filters iteratively adjust their coefficients to minimize the error between the desired clean ECG signal and the filtered output. The LMS filter's efficiency depends on parameters such as filter length, step size, and convergence criteria. In real-time applications, such as continuous monitoring, the filter must operate with low latency while adapting to dynamic ECG changes. Additionally, evaluating filter performance using metrics like Mean Squared Error (MSE) and Signal-to- Noise Ratio (SNR) ensures optimal noise reduction. Ultimately, an effective LMS filter can outcomes'. essential step -size LMS to computational costs essential monitoring systems health ecg-based lms filter.

II. EXISTING METHOD

ECG signals are essential for monitoring heart conditions, but they often get contaminated by various noise types, making it harder to analyze them accurately. Common noise sources include baseline wander (due to respiration and skin impedance) and high- frequency noise (from power lines, muscle artifacts, or poor electrode contact). To mitigate these issues, existing systems use digital filtering techniques, especially the Least Mean Squares (LMS) adaptive filter. While LMS filters are effective, they pose challenges in terms of power consumption, area usage, and processing delays.

Efficient hardware implementations are needed to overcome these limitations.

Crucial to the development of next-generation ECG noise reduction systems. By focusing on optimizing hardware components like adders and multipliers, and employing techniques such as approximate computing and algorithm-level enhancements, it's possible to reduce power consumption, improve speed, and reduce area usage.

This optimization will help make portable ECG devices more effective, compact, and power-efficient, which is essential for real-time monitoring.

Ultimately, these innovations will support the goal of providing high-quality, continuous ECG data for accurate and timely cardiac diagnoses, even in resource-constrained environments.

Table 1
Sources of Noise in ECG Signals

Noise Type	**Source**
Baseline Wander	Respiration, ski n impedance
High-Frequency Noise	Powerline interference, muscle artifacts, electrode contact noise

Table 2
Digital Filtering Techniques

Filter Type	**Features**
FIR Filters	Linear phase, guaranteed stability
Adaptive Filters	Dynamically adjusts to signal changes

Existing methodologies for ECG noise reduction provide a solid foundation, but they are hindered by several key limitations that require further research and optimization.

One major issue is the high transistor count and area consumption of traditional adder and multiplier implementations, particularly when larger bit-widths are necessary for high-precision processing.

This leads to increased chip area and cost, which is problematic for miniaturized portable ECG devices. Additionally, power inefficiency remains a significant challenge, as multipliers are known to be power-hungry, and their widespread use in LMS filters can significantly impact battery life in portable devices

Current designs often prioritize speed over power efficiency, resulting in higher energy consumption. Furthermore, the iterative nature of the LMS algorithm and the inherent delays in conventional adder and multiplier architectures can introduce processing latency, complicating real-time noise reduction. These drawbacks highlight the need for more advanced techniques to optimize both performance and efficiency in ECG noise reduction. Current ECG noise reduction systems, though functional, face significant challenges in achieving an ideal balance between performance and efficiency. The iterative nature of the LMS algorithm and the complexity of traditional hardware implementations of adders and multipliers underscore the need for more efficient designs that prioritize space and energy savings. To address these challenges, researchers are investigating approximate computing. where minor errors are deliberately introduced to reduce power, area, and processing time, thus improving overall efficiency. Additionally, efforts are focused on optimizing the LMS algorithm itself through techniques such as sparse adaptive filters, which reduce computational load by using only a subset of coefficients, and variable step-size LMS. which dynamically adjusts the step size to enhance convergence speed and reduce steady-state errors. Emerging technologies, including memristors and spintronic devices, hold great promise for developing ultra-low-power, high-density adaptive filters that could significantly improve ECG monitoring systems. These innovations could lead to the creation of portable, real-time ECG devices, offering the potential for early, accurate diagnoses and revolutionizing cardiac healthcare. one of the biggest advantages of the LMS algorithm is its suitability for real-time ECG signal processing, especially in wearable or portable healthcare devices. Due to its low computational complexity, LMS can be implemented on digital signal processors (DSPs), microcontrollers, or even FPGAs for real-time noise cancellation.

A. FIR Filter

An N-tap FIR (Finite Impulse Response) filter is a type of digital filter that uses a fixed number of past input values called taps to produce each output sample. Each tap corresponds to a delayed version of the input signal, multiplied by a specific coefficient. These weighted values are then summed to generate the output.

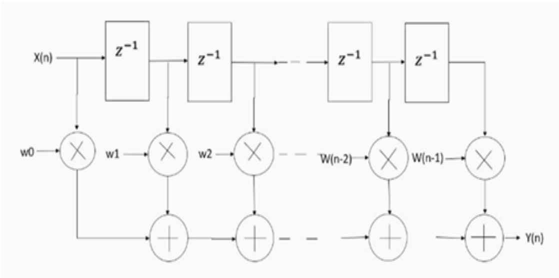


Fig. 1. N-tap FIR filter

Common noise sources include baseline wander (due to respiration and skin impedance) and high- frequency noise (from power lines, muscle artifacts, or poor electrode contact). To mitigate these issues, existing systems use digital filtering techniques, especially the Least Mean Squares (LMS) adaptive filter.

While LMS filters are effective, they pose challenges in terms of power consumption, area usage, and processing delays.

B. Adaptive LMS Filter

adaptive LMS Least Mean Squares filter is a type of adaptive filter that adjusts its filter coefficients automatically to minimize the error between the desired signal and the actual output. It uses the LMS algorithm, which is based on a simple and efficient gradient descent method.

The updates its weights by using the error signal the difference between the desired and the output signal to iteratively adapt to changing signal conditions.

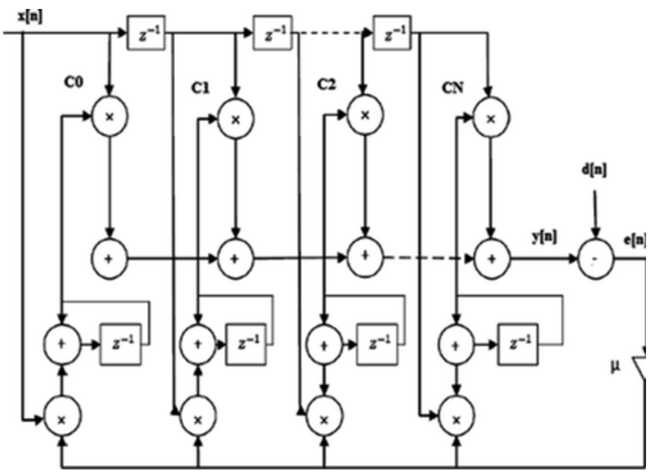


Fig. 2. N-tap LMS filter

C. 8X1 multiplexer full adder

A Full Adder can be implemented using an 8×1 multiplexer by utilizing the multiplexer's ability to select one of eight inputs based on three select lines. Since a full adder has three inputs—A, B, and Cin—these can be directly used as the select lines of the 8×1 MUX. The sum and carry outputs

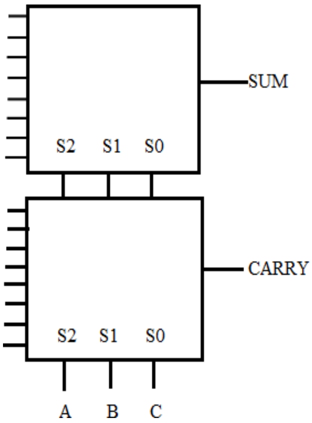


Fig .3. 8x1 multiplier full adder

are determined by the truth table of a full adder, which defines the output for all eight possible combinations of the three inputs. For the sum output, the logic is A ⊕ B ⊕ Cin, and for the carry output, the logic is AB + BCin + ACin. assigning the appropriate binary values (0 or 1) to the MUX inputs (I0 to I7) according to the truth table of sum and carry respectively, the multiplexer can generate the correct outputs. This method provides a systematic way of This optimization will help make portable ECG devices more effective, compact, and power-efficient, which is essential for real-time monitoring.

Crucial to the development of next-generation ECG noise reduction systems. By focusing on optimizing hardware components like adders and multipliers, and employing techniques such as approximate computing and algorithm-

Ultimately, these innovations will support the goal of providing high-quality, continuous ECG data for accurate and timely cardiac diagnoses, even in resource-constrained environments.

Table 1: Sources of Noise in ECG Signals

Noise Type	**Source**
Baseline Wander	Respiration, skin impedance
High-Frequency Noise	Powerline interference, muscle artifacts, electrode contact noise

Table2:Digital Filtering Techniques

Filter Type	**Features**
FIR Filters	phase, guaranteed stability Linear

Existing methodologies for ECG noise reduction provide a solid foundation, but they are hindered by several key limitations that require further research and optimization.

One major issue is the high transistor count and area implementations, particularly when larger bit-widths are necessary for high-precision processing.

This leads to increased chip area and cost, which is problematic for miniaturized portable ECG devices. Additionally, power inefficiency remains a significant challenge, as multipliers are known to be power-hungry, and their widespread use in LMS filters can significantly impact battery life in portable devices

Current designs often prioritize speed over power efficiency, resulting in higher energy consumption.

Furthermore, the iterative nature of the LMS algorithm and the inherent delays in conventional adder and multiplier architectures can introduce processing latency, complicating real-time noise reduction.

These drawbacks highlight the need for more advanced techniques to optimize both performance and efficiency in ECG noise reduction.

Current ECG noise reduction systems, though functional, face significant challenges in achieving an ideal balance between performance and efficiency.

where minor errors are deliberately introduced to reduce power, area, and processing time, thus improving overall efficiency. Additionally, efforts are focused on optimizing the LMS algorithm itself through techniques such as sparse adaptive filters, which reduce computational load by using only a subset of coefficients, and variable step-size LMS.

which dynamically adjusts the step size to enhance These innovations could lead to the creation of portable, real-time ECG devices, offering the potential for early, accurate diagnoses and revolutionizing cardiac healthcare.

III. PROPOSED METHOD

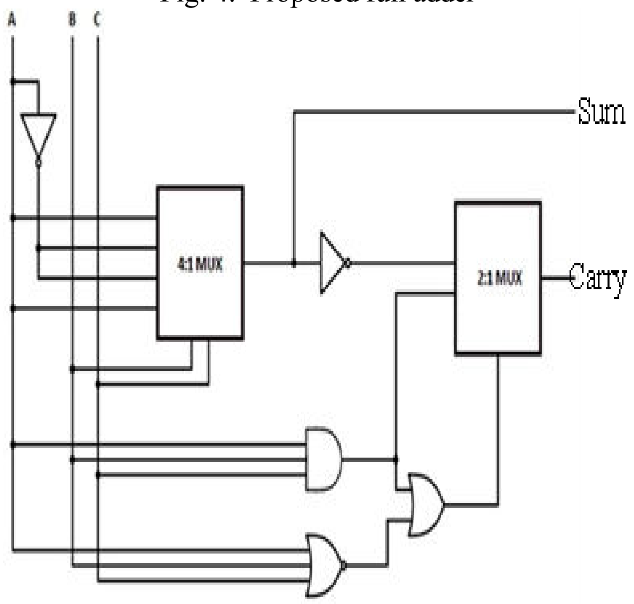
The proposed design introduces a more efficient 4:1 multiplexer-based full adder in place of the traditional 8:1 multiplexer.

This seemingly small change leads to several benefits, including a reduced transistor count, simplified logic, and lower power consumption.

A. Proposed full adder

consumption of traditional adder and multiplier the proposed full adder refers to a modified or optimized version of the traditional full adder circuit, designed to improve performance in terms of speed, area, or power consumption. In digital electronics, a standard full adder adds three input bits—A, B, and Cin—and produces a Sum and a Carry output

Fig. 4. Proposed full adder



B. Ripple carry adder

A ripple carry adder is a type of digital circuit used for binary addition. It consists of a series of full adders, each of which adds two input bits and a carry bit from the previous stage. The name "ripple carry" comes from the way the carry output from each full adder is passed (or "ripples") to the next one in the sequence.

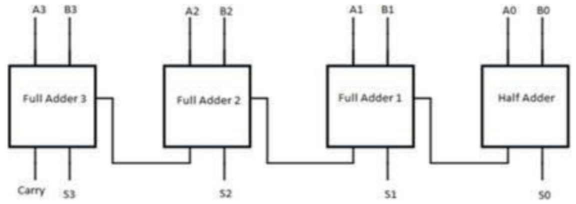


Fig.5. Designed ripple carry adder

The use of multiplexers (MUX) in the adder design makes it more efficient by reducing complexity and minimizing errors.

Additionally, the design is implemented using Verilog HDL, ensuring scalability, flexibility, and rigorous simulation for functional verification. This optimized approach contributes to a more power-efficient and compact design suitable for portable ECG monitoring devices. Current ECG noise reduction systems face challenges in balancing performance and efficiency.

C. Multiplier

multiplier is a digital circuit used to perform multiplication of two binary numbers. It takes two input binary numbers usually called the multiplicand and the multiplier and produces an output which is their product.

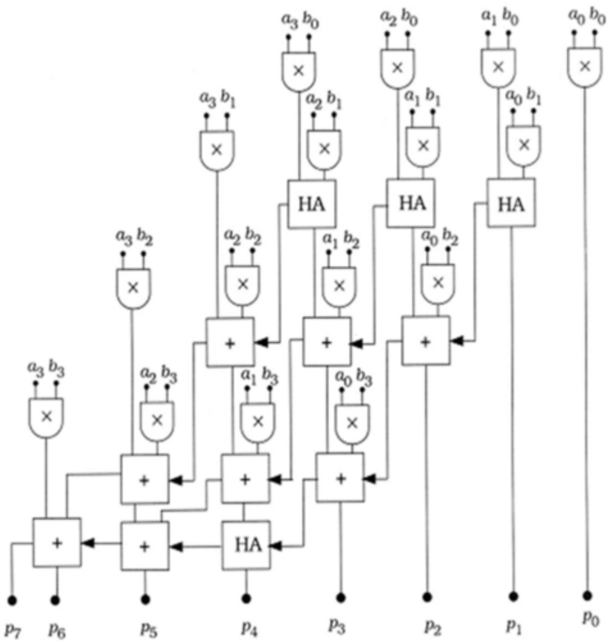


Fig.6. Designed Multiplier

D.FIR Filter

A FIR (Finite Impulse Response) filter is a type of digital filter used in signal processing to manipulate or enhance signals. The term "finite impulse response" means that the filter's response to an impulse (a very short signal) settles to zero in a finite amount of time. FIR filters work by taking a finite number of past input values, multiplying them by fixed coefficients (called filter taps), and summing the results to produce the output.

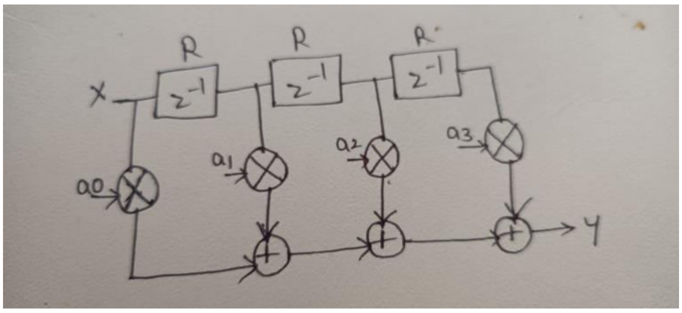


Fig.7.Designed multiplier

The iterative nature of the LMS algorithm, combined with the complexity of traditional hardware components like adders and multipliers, results in high power consumption, large area usage, and increased latency.

These limitations make it difficult to integrate such systems into portable, real-time ECG monitoring devices, hindering their effectiveness in critical, time-sensitive cardiac applications.

Optimization in hardware design is necessary to meet the demands of real-time monitoring while reducing power consumption and area requirements.

An easy way to comply with the conference paper formatting requirements is to use this document as a template and simply type your text into it. The proposed design replaces the traditional 8:1 multiplexer full adder with a more efficient 4:1 multiplexer-based version. This change reduces transistor count, simplifies logic, and lowers power consumption. Using multiplexers in the design decreases complexity and minimizes errors. The design is implemented in Verilog HDL, ensuring flexibility, scalability, and thorough verification, making it a more power-efficient and compact solution for portable ECG devices.

E. LMS Filter

A 4-tap LMS (Least Mean Squares) filter is an adaptive digital filter with four taps, meaning it uses four past input samples to compute the output. The LMS filter is designed to minimize the error between the desired signal and the actual filter output by adjusting its coefficients (weights) dynamically using the LMS algorithm.

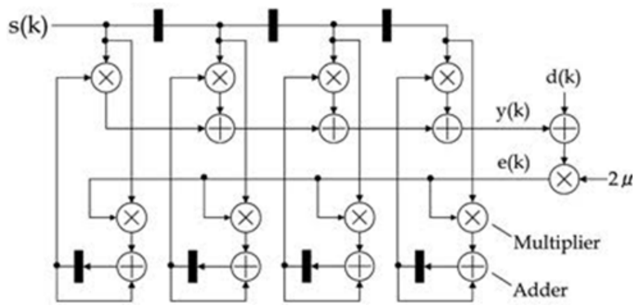


Fig.8.4-Tap LMS filter

Array multipliers are simple circuits that multiply numbers using a grid of AND gates and adders, but they can be slow and inefficient for larger numbers. Booth multipliers, on the other hand, speed up the process by reducing the number of partial products, making them more power-efficient. Wallace tree multipliers use a tree structure to quickly add partial products, improving speed. The Least Mean Squares (LMS) algorithm is used in signal processing to minimize errors by adjusting filter settings. An Electrocardiogram (ECG) records the heart's electrical activity, and FIR filters process signals using a limited number of previous inputs to remove noise and improve clarity.

Wearable devices face several challenges when integrating complex arithmetic units, such as multipliers, which can hinder their performance and practicality.

One major issue is the high area consumption associated with large transistor counts, making it difficult to miniaturize these components for use in compact wearable devices.

This increases both the size and cost of the devices, limiting their feasibility. Additionally, excessive power consumption is a significant concern, particularly for multipliers, which are power-hungry .

The use of multiplexers (MUX) in the adder design makes it more efficient by reducing complexity and minimizing errors.

Additionally, the design is implemented using Verilog HDL, ensuring scalability, flexibility, and rigorous simulation for functional verification. This optimized approach contributes to a more power-efficient and compact design suitable for portable ECG monitoring devices. Current ECG noise reduction systems face challenges in balancing performance and efficiency.

The iterative nature of the LMS algorithm, combined with the complexity of traditional hardware components like adders and multipliers, results in high power consumption, large area usage, and increased latency.

These limitations make it difficult to integrate such systems into portable, real-time ECG monitoring devices, hindering their effectiveness in critical, time-sensitive cardiac applications.

Optimization in hardware design is necessary to meet the demands of real-time monitoring while reducing power consumption and area requirements.

An easy way to comply with the conference paper formatting requirements is to use this document as a template and simply type your text into it.

the proposed design replaces the traditional 8:1 multiplexer full adder with a more efficient 4:1 multiplexer-based version.

This change reduces transistor count, simplifies logic, and lowers power consumption. Using multiplexers in the design decreases complexity and minimizes errors.

The design is implemented in Verilog HDL, ensuring flexibility, scalability, and thorough verification, making it a more power-efficient and compact solution for portable ECG devices.

This increases both the size and cost of the devices, limiting their feasibility. Additionally, excessive power consumption is a significant concern, particularly for multipliers, which are power-hungry components.

This results in shorter battery life, making continuous monitoring difficult and limiting the device's long-term usability. Array multipliers are simple circuits that multiply numbers using a grid of AND gates and adders, but they can be slow and inefficient for larger numbers. Booth multipliers, on the other hand, speed up the process by reducing the number of partial products, making them more power-efficient. Wallace tree multipliers use a tree structure to quickly add partial products, improving speed. The Least Mean Squares (LMS) algorithm is used in signal processing to minimize errors by adjusting filter settings. An Electrocardiogram (ECG) records the heart's electrical activity, and FIR filters process signals using a limited number of previous inputs to remove noise and improve clarity. Wearable devices face several challenges when integrating complex arithmetic units, such as multipliers. which can hinder their performance and practicality. One major issue is the high area consumption associated with large transistor counts, making it difficult to miniaturize these components for use in compact wearable devices. This increases both the size and cost of the devices, limiting their feasibility. Additionally, excessive power consumption is a significant concern, particularly for multipliers, which are power-hungry co combination of 4:1 and 2:1 multiplexers along with basic logic gates like AND, OR, and NOT, which reduces the potential for errors during implementation. Third, the reduction in the number of transistors and simplified circuit design directly lowers power consumption, making the system more energy-efficient, an important factor for modern devices.

Table 1: Challenges in Current ECG Noise Reduction Systems

Challenges	Description
High Area Consumption	Large transistor counts limit miniaturization, increasing cost and space requirements.
Excessive Power Consumption	Multipliers are power-hungry, reducing battery life and limiting contimonitoring.

IV. RESULTS AND DISCUSSION

Electrocardiogram (ECG) signals are often corrupted by various types of noise, including power line interference, baseline wander, muscle artifacts, and electrode motion artifacts. An Adaptive Least Mean Squares (LMS) Filter is a widely used technique for noise reduction in ECG signals due to its ability to adaptively adjust filter coefficients to minimize the error signal.

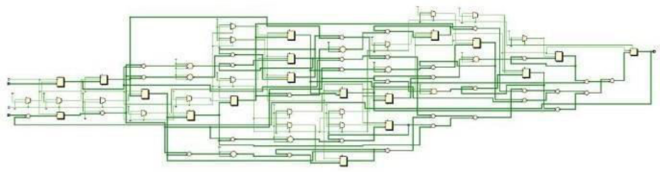
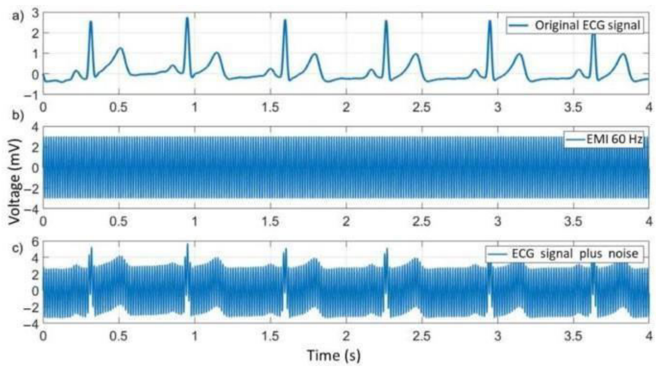


Fig 1: RTL Schematic diagram

ECG Signal:



Power consumption

The power line interference from ECG signal can be removed by adaptive filtering while it's harmonics and high frequency noise can be removed by implementing general notch rejection filter.

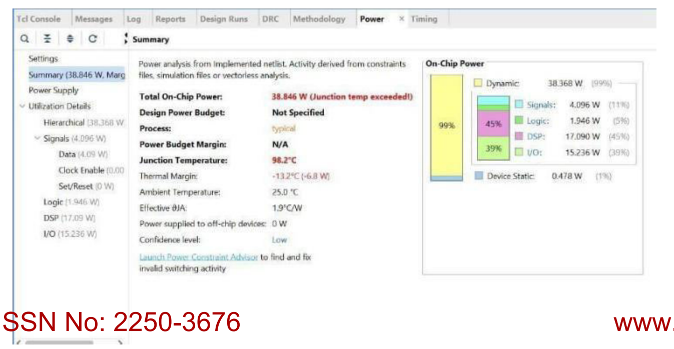


Fig 2: power consumption

This graph shows the resource utilisation after synthesis and implementation. Interesting, the IO utilisation is the highest.

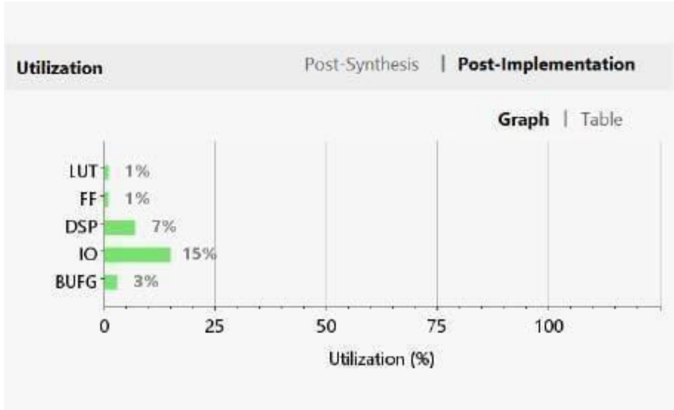
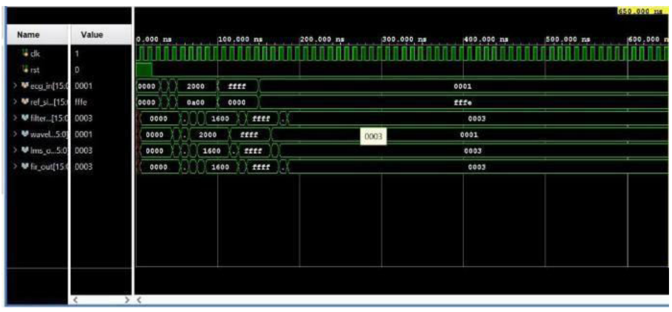


Fig 3: Utilization

Fig 4: Simulation Results



V. CONCLUSION

An adaptive LMS filter was developed to reduce noise in ECG signals, effectively addressing baseline drift and high-frequency interference, thereby enhancing the accuracy of cardiac diagnosis using ECG data. The filter was implemented in Xilinx Vivado version 2021.2, utilizing a custom adder and multiplier design that incorporated basic gates, a 2x1 MUX, and a 4x1 MUX. The results showed that the proposed design led to a 5.53% reduction in power consumption and a 4.48% decrease in area compared to the existing adaptive LMS filter with conventional adders and multipliers. This advancement holds significant potential to improve hardware performance in both cardiac diagnostics and clinical applications

VI. REFERENCES

[1] B. Boro, K. M. Reddy, Y. N. Kumar and M. H. Vasantha, "Approximate radix-8 Booth multiplier for low-power and high-speed applications," *Microelectronics Journal,* Vol. 101, no. 8, pp. 604-816, Jul. 2020, doi: 10.1016/j.mejo.2020.104816.

[2] M. Yamini Divya and B. K. L. Aruna, "Implementation of 32-Bit Adders using Different Full Adders," *International Journal of Engineering Research & Technology,* Vol. 9, no. 6, pp. 743-845, Oct. 2020.

[3] Y. Du, Z. Chen, B. Cheng and W. Shan, "Design and analysis of leading one/zero detector-based approximate multipliers," *Microelectronics Journal,* Vol. 136, no. 7, pp. 105-783, Jun. 2023, doi: 10.1016/j.mejo.2023.105783.

[4] M. M. U. Faiz and I. Kale, "Removal of multiple artifacts from ECG signal using cascaded multistage adaptive noise cancellers," *Journal of Array,* Vol. 14, no. 1, pp. 100-133, Jul. 2022, doi: 10.1016/j.array.2022.100133.

[5] S. E. Fatemieh, S. S. Farahani, and M. R. Reshadinezhad, "Low-power, area-efficient, and high-performance approximate full adder based on static CMOS," *Sustainable Computing: Informatics and Systems,* Vol. 30, no. 4, pp. 100-529, Jun. 2021, doi: 10.1016/j.suscom.2021.100529.

[6] S. Janwadkar and R. Dhavse, "Power and area efficient FIR filter architecture in digital encephalography systems," *e-Prime-Advances in Electrical Engineering, Electronics and Energy,* Vol. 4, no. 9, pp. 100148, Jun. 2023, doi: 10.1016/j.prime.2023.100148.

[7] H. Jiang, J. Han, F. Qiao and F. Lombardi, "Approximate radix-8 booth multipliers for low- power and high-performance operation," *IEEE Transactions on Computers,* Vol. 65, no. 8, pp. 2638-2644, Aug. 2016, doi: 10.1109/TC.2015.2493547.

[8] J. Kandpal, A. Tomar, M. Agarwal and K. Sharma, "High-speed hybrid-logic full adder using high-performance 10-T XOR–XNOR cell," *IEEE Transactions on Very Large Scale Integration Systems,* Vol. 28, no. 6, pp. 1413-1422, Jun. 2020, doi: 10.1109/TVLSI.2020.2983850.

[9] K. C. Kuo and C. W. Chou, "Low power and high-speed multiplier design with row bypassing and parallel architecture," *Microelectronics Journal,* Vol. 41, no. 10, pp. 639-650, Oct. 2010, doi: 10.1016/j.mejo.2010.06.009.

[10] P. Kumar a n d R. K. Sharma, " Low voltage high performance hybrid full adder," *Engineering Science and Technology, an International Journal,* Vol. 19, no. 1, pp. 559-565, Mar. 2016, doi: 10.1016/j.jestch.2015.10.001.

[11] P. Patali and S. T. Kassim, "Efficient modular hybrid adders and Radix-4 booth multipliers for SP applications," *Microelectronics Journal,* Vol. 96, no. 3, pp. 104-701, Feb. 2020, doi: 10.1016/j.mejo.2020.104701.

[12] N. M. Priya, C. B. Thangammal, R. Seshasayanan and S. Radley, "High-performance fir filter based on Vedic mathematic," *International Journal of System Assurance Engineering and Management,* Vol. 142, no. 8, pp. 581-697, Apr. 2023, doi: 10.1007/s13198-023-01899-z.

[13] A. Rajput, T. Dua, R. Kumawat and A. Srinivasulu, "Half Adder using Different Design Styles: A Review on Comparative Study," *Journal of Advancements in Robotics,* Vol. 7, no. 3, pp. 26-32, 2020.

[14] M. Saritha, K. Chaitanya, V. Vijay, A. Aishwarya, H. Yadav and G. D. Prasad, "Adaptive and recursive Vedic kara tsuba multiplier using non-linear carry select adder," *Journal of VLSI circuits and systems,* Vol. 4, no. 2, pp. 22-29, Mar. 2022, doi: 10.31838/jvcs/04.02.04.

[15] R. Sakthivel and G. Ragunath, "Low power area optimized and high speed carry select adder using optimized half sum and carry generation unit for FIR filter," *Journal of Ambient Intelligence and Humanized Computing,* Vol. 12, no. 9, pp. 5513-5524, May. 2020, doi: 10.1007/s12652-020-02062-3.

[16] H. Sohal and S. Jain, "FPGA implementation of collateral and sequence pre-processing modules for low-power ECG denoising module," *Informatics in Medicine Unlocked,* Vol. 28, no. 6, pp. 100-238, Jan. 2022, doi: 10.1016/j.imu.2021.100838.

[17] G. Swaminathan, G. Murugesan, S. Sasikala and L. Murali, "A novel implementation of combined systolic and folded architectures for adaptive filters in FPGA," *Microprocessors and Microsystems,* Vol. 74, no. 7, pp. 103-218, Apr. 2020, doi: 10.1016/j.micpro.2020.103018.