"Design and Analysis of Clock-Gated Domino Logic for Power Reduction in 16 nm CMOS"

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Abstract—

In this paper, a new technique of power reduction in a cmos domino logic is proposed. The proposed technique uses clock gating as well as output hold circuitery. Clock is passed to the domino logic only during the active state of the circuit. During standby mode, clock is bypassed while the state of the circuit is retained. A 2:1 multiplexer is used for clock gating and for retaining the state of the circuit. Simulation results are being carried out in a 2-input nand gate, 2-input nor gate and 1-bit conventional full adder cell in 16nm cmos technology. The power of the proposed circuit is reduced to an average of 99.37 percent with respect to standard domino logic. Propagation delay is slightly increased to an average of 4.53 percent. Area of the proposed circuit increases to four transistors per domino module.

Index Terms—Dynamic, Domino, static power, clock gating, cmos

I. Introduction

To achieve higher performance of the cmos device circuit along with high densities, there have been reductions in supply voltages, device dimensions and transistor threshold voltages over the years. But, these reductions have also resulted in higher leakage currents that can severely affect power consumption in a circuit. The power comsumption of any cmos VLSI circuit is composed of dynamic power and static power. The dynamic power dissipation is due to the switching activities of the circuit while the static power dissipation occurs due to the leakage components of the circuit during the standby mode. During sub-micron technology when the feature size was greater than 350nm, the leakage power
dissipation was smaller than dynamic power by several orders of magnitude [1]. With technology scaling there is a need of lowering of supply voltage and threshold volatge of VLSI circuits. However lowering of threshold volatge increases the static power dissipation. In ultra-deep sub-micron technology where the feature size is lesser than 100nm, static power dissipation has dominated the dynamic power. Thus there is need for reducing the static power dissipation in ultra-deep sub-micron technology.
Domino Logic has proved to be a useful circuit in VLSI technology. Domino logic has various advantage like small area and high speed operation as compared to its static cmos counterparts [2]. It uses the best property of static and dynamic logic without suffering from the load capacitance sensitivity as in pure dynamic logic [3]. Domino logic is a clocked logic family which means that there is a clock in every logic gate. The continous switching of clock in domino logic design leads to the higher power dissipation. Many techniques have been proposed to lower the power dissipation in domino logic module like scaling the supply voltage [4] or using low-swing clock [5] but a little focus has been given to clock gating technique. A clock gating technique have been used in [6] which uses clock enabler ciruit.

A. Contribution

In this paper, a clock gating technique is applied during the static mode of the domino logic which significantly reduces the static power dissipation to an average of 99.37 percent as compared to the standard domino logic module. The state of the circuit is retained during standby mode. A little loss in performance of up-to 4.53 percent is recorded during the simulation. Thus the proposed design is suitable for low power applications.

II. Operation of Domino Logic

A domino logic module consist of a pull down network (PDN), dynamically connected, followed by a static inverter [7] as shown in figure 1. The non-inverting output of domino is represented by signal *out* while domino node is represented by *X*. The PDN is built exactly as that in complementary cmos. The domino module works in two phases - *precharge* and *evaluation*, where the signal *clock* controls the mode of operation as shown below:

$$clock = \begin{cases} 0, & \text{precharge phase} \\ 1, & \text{evaluation phase} \end{cases} \quad (1)$$

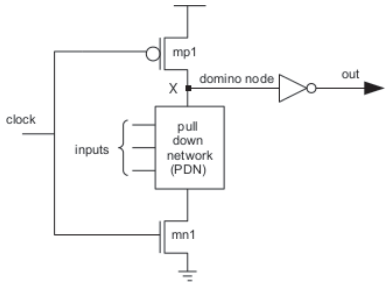

Fig. 1. A Standard Domino Logic Module

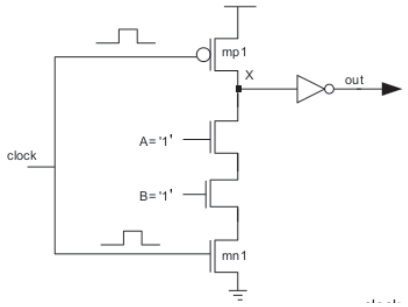

Fig. 2. Nand gate using domino logic

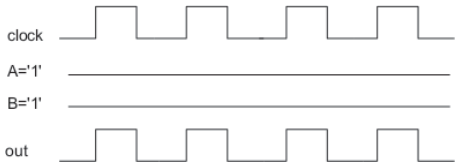

Fig. 3. Waveforms for a 2-input nand gate using domino logic during standby mode

During *precharge* phase, domino node *X* is charged to V_{DD} by pmos transistor *mp1*. The nmos transistor *mn1* is *off* during this phase. During *evaluation* phase, transistor *mp1* is *off* while *mn1* is in *on* state. If the input values are such that PDN conducts, node *X* discharges, otherwise it will hold the precharge value i.e. V_{DD}.

Figure 2 shows the domino logic module for a 2-input *nand* gate. Let the inputs of a 2-input *nand* gate domino logic are *'11'* i.e. *A='1'* and *B='1'* during standby mode. For this case, the *out* should be *'1'* but since the clock is present, *out* is a pulse as shown in figure 3. The presence of clock and the pulse shaped output dissipates a significant amout of power dissipation during standby mode. For the other combinations of standby inputs i.e. *'00, '01' and '10'*, *out* is '0'. The presence of clock in domino logic leads to power dissipation in this case.

Domino logic is faster than its static logic counterparts. Although, it is very sensitive to noise sources such as leakage current, crosstalk, charge sharing, power supply bump and ground bounce since its dynamic node can not be recovered after the data is lost by those noise sources [8].

III. Proposed Technique

The proposed design uses clock gating in order the pass the clock only during the active state of the circuit. During standby mode, when the inputs of PDN are not changing, clock is not passed to the domino module and the output value of the circuit is hold till the next input transition. Figure 4 shows the proposed design of the domino cmos logic. Here, a 2:1 multiplexer, mux, is used for clock gating and output hold. Signal *clock* and *output* are the inputs of mux while *y* is the output. The *sleep* is the control signal of mux. The output of mux i.e. signal *y* is as follows:

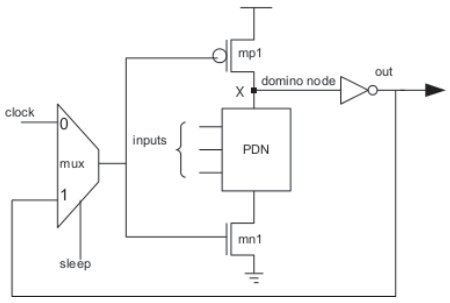

Fig. 4. Proposed design for domino logic

$$y = \begin{cases} clock, & \text{if } sleep =^{J} 0^{J} \\ output, & \text{if } sleep =^{J} 1^{J} \end{cases} \quad (2)$$

The value of signal *sleep* is as follow:

$$sleep = \begin{cases} '0' & \text{for active mode} \\ '1' & \text{for standby mode} \end{cases} \quad (3)$$

A. Operation of the Proposed Domino Logic

When the inputs of pull-down-network (PDN) are changing and circuit is in active mode, the signal *sleep* is '0' and *y = clock*. The *clock* signal passes to mp1 and mn1 transistors and operates the standard domino logic functionality. When the inputs are not changing, the signal *sleep* is '1' while *y = out*. This will hold the circuit state as explained below.

Let *out* $=^{J} 1^{J}$ during standby mode. This means that domino node *X* $=^{J} 0^{J}$. Thus PDN is in conducting mode. Now, let *sleep* changes from '0' to '1'. Signal *y* will thus changes from *clock* to *out* i.e '1'. Thus mn1 is *on* while *mp1* is *off*. Since PDN is already in conducting mode, the domino node becomes '0' while the value *out* $=^{J} 1^{J}$ is retained. Figure 5 shows the domino logic with clock gating during standby mode and *out* $=^{J} 1^{J}$. Figure 6 shows the waveform of the proposed design for a 2-input *nand* gate for *A='1', B='1'* and *sleep* signal changing from '0' to '1'. It can be seen that as the sleep signal becomes '1', *out* stops oscillating preventing the power dissipation.

Let *out* is '0' during standby mode. This means *X* $=^{J} 1^{J}$. Thus PDN is not conducting. Let *sleep* changes from '0' to '1'. Now the values of *y* will also changes from *clock* to *out* i.e '0'. The value *y* $=^{J} 0^{J}$ puts mn1 to *off* state while *mp1* is *on*. Thus *X* charges to V_{DD} retaining the state of the circuit.

In the proposed design, neither the clock is present in the domino module during standby mode, nor the output oscillates preventing the power dissipation in the circit.

B. Multiplexer Design

Here, a 2-input multiplexer is used for selecting one out of two inputs i.e. *clock* or *out*. The multiplexer is designed using transmission gates which combines the complementary

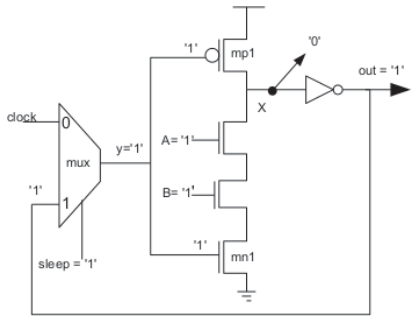

Fig. 5. Proposed design for a 2-input *nand* gate during standby mode with *out='1'*

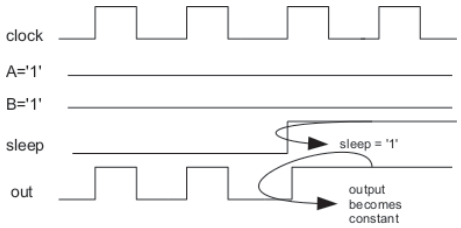

Fig. 6. Waveforms for a proposed 2-input *nand* gate during standby mode

properties of nmos and pmos transistors [7]. The nmos transistor passes a weak '1' but a good '0' while pmos passes a good '1' and weak '0'. Figure 7 shows the multiplexer using transmission gates used in the proposed design. Figure 8 shows the proposed design for a 1-bit conventional full adder domino logic.

C. Results and discussions

Ngspice simulator is used for simulating purpose. The 16nm PTM (*predictive technology model*) model are used to simulate the domino logic and the proposed technique. The threshold voltage for nmos transistor is 0.48V while for pmos transistor is -0.43V. Supply voltage, V_{DD} is taken as 0.9V. Width of the

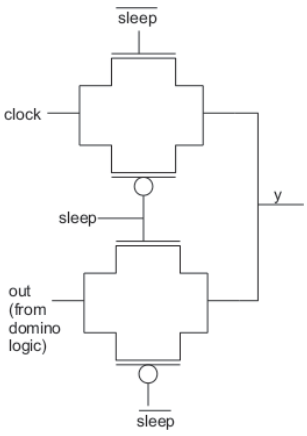

Fig. 7. A 2:1 multiplexer used in the proposed design

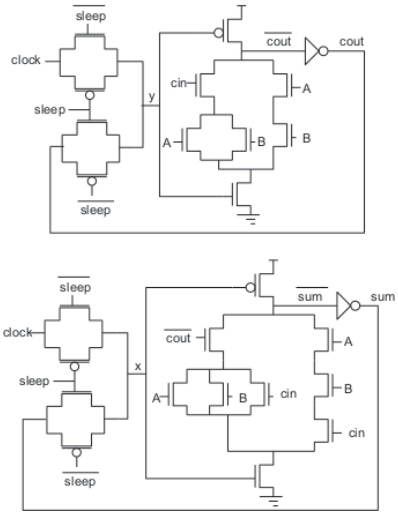

Fig. 8. A 1-bit conventional full adder circuit using proposed design

TABLE I
RESULTS for DOMINO LOGIC

Circuit	Static Power *(μW)*	Dynamic Power *(fW)*	Delay *(ns)*
NAND gate	1.58	0.49	4.22
NOR gate	6.25	1.30	4.22
Full Adder	3.27	0.82	3.72

pmos transistor is 2.5 times the width of nmos transistor. A 2-input *nand* gate, 2-input *nor* gate and and 1-bit conventional full adder are taken as the verifying circuits.

Table I shows the values of static power, dynamic power and delay for 2-input *nand* gate, 2-input *nor* gate and 1-bit conventional full adder circuits designed using domino technology. Table II shows the values of results of proposed technology. Table III shows the comparison of proposed logic with respect to domino logic. The units *fW*, *nW*, *μW* and *ns* represents *femto-watts*, *nano-watts*, *micro-watts* and *nano-secs* respectively. The negative values of static power in the table III shows that the static power of proposed is reduced with respect to domino logic. Similary the positive perentage implies the increase in delay in proposed logic with respect to domino. Figure 9, 10 and 11 shows the charts for static power, dynamic power and delay respctively for domino and proposed logic. It can be clearly seen form all the above tables and charts that the proposed logic i.e. domino with clock gating and output hold circuit reduces the static power by approximately 99 percent in all the cases with a small increase of approximately 4.5 percent in delay. There is no change in dynamic power and it is approximately constant in all the cases. There is a increase in area of four transistors per domino cell.

IV. Conclusion

A clock gating scheme is applied to the standard domino logic which will bypass the clock during the standby mode of the circuit and will retain the circuit state. A 2:1 multiplexer

TABLE II
RESULTS for PROPOSED LOGIC

Circuit	Static Power *(nW)*	Dynamic Power *(fW)*	Delay *(ns)*
NAND gate	20.1	0.49	4.43
NOR gate	11.6	1.30	4.42
Full Adder	10.2	0.82	3.87

TABLE III
COMPARISON of PROPOSED LOGIC w.r.t DOMINO LOGIC

Circuit	Static Power	Delay
NAND gate	-98.70%	+4.90%
NOR gate	-99.80%	+4.70%
Full adder	-99.60%	+4.00%

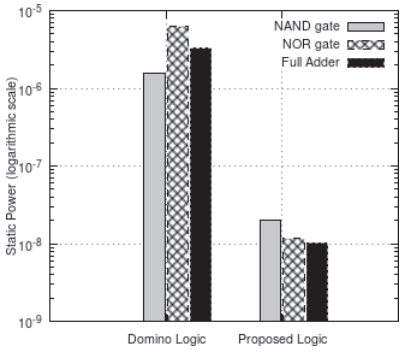

Fig. 9. Static Power for Domino and Proposed logic

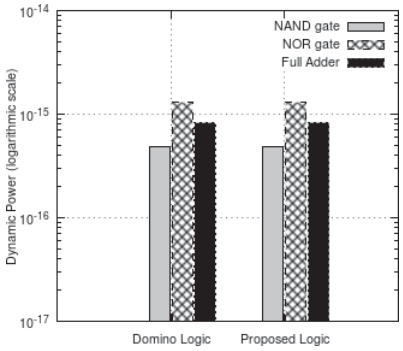

Fig. 10. Dynamic Power for Domino and Proposed logic

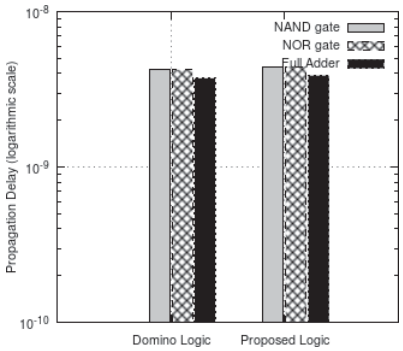

Fig. 11. Propagation Delay for Domino and Proposed logic

using transmission gates is used for applying clock gating with output hold circuity. There is an improvement of 99.37 percent in static power dissipation in the proposed logic with respect to standard domino logic. There is small increase in delay of 4.53 percent in proposed logic with respect to domino logic. Thus proposed domino logic is a very low power design in ultra-deep sub-micron technology. This design dissipates less amount of power with some loss in performance. Low power devices has the feature of dissipating low power with increased delay. Thus this device is suitable for low power devices.

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