Design and Implementation of High-Speed, Low- Power CMOS D Flip-Flop and Counters using Double Gate FinFET Technology

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Abstract— As Semiconductor technology advances, there is a growing demand for energy-efficient digital circuits in various applications, including portable devices and data centers. FinFET (Fin Field Effect Transistor) technology has emerged as a promising solution to meet these demands. FinFET technology, a leading innovation in the semiconductor industry, is known for its capability to deliver exceptional performance and energy efficiency. This paper provides an overview of the designing and simulation of counter using 10nm FinFET technology in LT-spice, a popular electronic circuit simulation tool. Conventional CMOS technology faces challenges related to short-channel effects as technology scales down, resulting in performance degradation. Power consumption and noise are reduced by 57.13%, 46.02% when counter are designed ,implemented with FinFET based D- Flip Flop. Inconstant, FinFETs offer superior resistance to short-channel effects and have emerged as a promising solution for advancing technology scaling. Finally, the results obtained from the proposed Jhonson Counter, asynchronous counters using FINFET are better when compared to Static CMOS Logic.

Keywords— CMOS, Counter, FinFET, Flip-flop, Short channel effect(SCE), True Single-Phase Clock (TSPC).

I. INTRODUCTION

Counters are indispensable building blocks of digital systems and are used in a wide range of electronic devices, starts from simple consumer gadgets to complex computing systems to perform the tasks such as counting events, generating timing signals, and implementing control logic. The performance and efficiency of these counters directly impact the overall functionality of the circuits they serve. All electronic circuits nowadays must have a low power consumption while increasing their operating speed. FinFET technology offers significant improvements in performance and energy efficiency, making it an ideal solution for digital counter design.

Researchers have employed various technologies to create circuits that use less power [1-3] and explored several methods for creating power-efficient D-Latches. The newly designed D-Latches use less power than the ones that are currently on the market 18nm FinFET technology was used to create these circuits provides a thorough analysis on behavioural characteristics of TSPC DFFs in relation to metastability. TSPC DFFs don't need any setup time but requires a much longer hold time [4-5]. An area-power-efficient shunt capacitor technique is utilized to significantly shorten the hold times with slightly lengthened setup times [6]. The Johnson Counter is a modified ring counter that made up of a sequence of flip-flops that can store binary information. In this counter design, the switched result produced by the final flip-flop is linked as a component of the initial flip-flop, creating a loop. This loop enables the Johnson Counter to generate a specific sequence of binary numbers when a clock signal is applied [7]. CMOS technology is prominent one for designing low power circuits where they consume power primarily during state transitions, and a very little amount of power in static states, making them energy efficient. One of the factors contributing to power dissipation in CMOS circuits is high leakage current as threshold voltage. This can be reduced by different approaches such as lowering supply voltage, Planar CMOS and FinFET structures [8 – 9].

This study intends to develop a high-speed, and low-power CMOS D flip-flop using Double Gate (DG) FinFET (Fin-shaped Field Effect Transistor) technology. The impact of W_{fin} scaling (down to below 10nm) on FinFET analog performance is investigated in this work. The findings show that decreasing the fin thickness in FinFETs does not significantly improve analog performance, instead, it causes a decline in the device transconductance (g_m) and output conductance (g_{ds}). Gm deterioration and gds improvement are also brought on by the decrease in W_{fin}. RS/D, ρ, and T are the main variables influencing gm variation in sub-10nm fin FinFETs. 4-bit Johnson and Ripple counters with a 1V supply voltage and 45nm technology are designed and implemented.

The following is a brief description of the paper: Section II includes implementation of counters; Section III discusses simulation results of the proposed designs; Section IV gives a conclusion and followed by references.

II. IMPLEMENTATION OF COUNTERS

The demand for efficient and high-performance execution of basic memory components, especially D Flip-

Flops, has increased in modern VLSI circuits. The D flip-flop is a fundamental component used for building memory elements in sequential digital circuits like registers, memory cells, other storage elements [10]. A Master-Slave D F/F is a type of sequential circuit composed of two separate D flip-flops, referred to as the master and slave sections which is shown in Fig.1. The purpose of using a master-slave configuration is to eliminate the possibility of race conditions that might occur in a single D flip-flop [11]. Table.1 shows behaviour of the D Flip Flop.

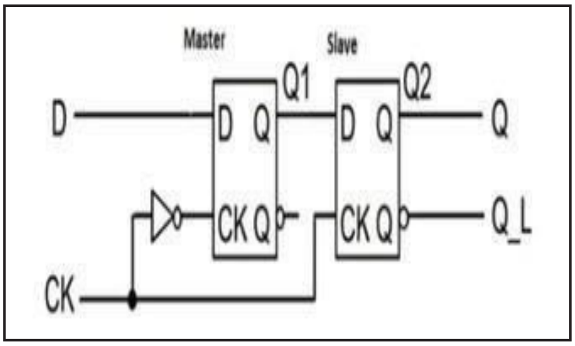

Fig. 1. Master Slave D flipflop

TABLE I. TRUTH TABLE OF D FLIPFLOP

D	Q(Current)	Q(n+1) (Next)
0	0	0
0	1	0
1	0	1
1	1	1

Flip-flop design is an electronic circuit that facilitates the storage of binary data. True Single-Phase Clock (TSPC) flip-flop, also known as a single transistor flip-flop, is a dynamic flip-flop design that employs a single transistor clocked by a short pulse train [12]. This design is widely used due to its ability to perform flip-flop operations rapidly and with minimal power consumption. TSPC is highly efficient in terms of both area and power consumption, making it a popular choice for various digital VLSI clocking systems, microprocessors, and buffer circuits. It operates on a single clock phase, which can be either the rising or falling edge of the clock signal, and is classified as an edge-triggered flip-flop. Due to its high speed and low power consumption, the TSPC is a flip-flop circuit that is mainly used in digital systems. The single-phase clock synchronization of this circuit removes the requirement for intricate clocking schemes. Through the use of TSPC, digital systems' performance can be significantly improved while requiring less space and enabling higher clock frequencies. Because of this, TSPC is frequently used in wireless communication systems, microprocessors, buffers, and digital VLSI clocking systems [13 – 14].

TSPC based D – flipflop design in H-spice is shown in fig.2. One significant benefit of the TSPC circuit design over other flip-flop circuits is that it simplifies the clock structure by using only one clock phase. The circuit's ability to store binary values and provide a dynamic latch function is what makes it so simple The inputs and outputs of the circuit are connected via a transistor-based network to accomplish this purpose. Furthermore, the TSPC can run at high speeds with minimal power consumption thanks to its dynamic operation. In conclusion, the TSPC circuit is a great option for use in digital systems due to its ease of use, high speed of operation, and low power consumption. Its efficacy in enhancing the performance of these systems is demonstrated by its use in digital VLSI clocking systems, microprocessors, buffers, and wireless communication systems.

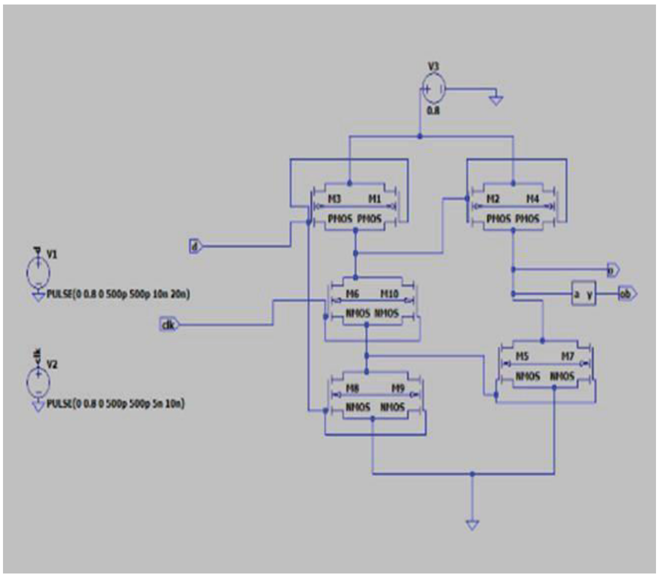

Fig. 2. TSPC based D – FlipFlop.

A. *Johnson Counter*

Since counters are typically built with traditional D, T, or JK flip flips, they frequently have power consumption issues. Not only do they use more power, but their designs are also more sophisticated. A low-power consumption flip flop was selected to make the design more power-efficient. There are four stages of cascaded D registers in the Johnson counter which is shown in Fig.3. Truth table of Johnson counter is represented in Table.2. With one clock and one input, a FinFET inverter and two D latches have been used to build the D register design. All of the flip flops receive the same clock input because it is synchronous[15-17]. A Johnson counter, also known as a switch tail ring counter, is a counter in which the reversed output of the final flip flop is fed back into the first flip flop of the Counter Designed this using LT-spice.

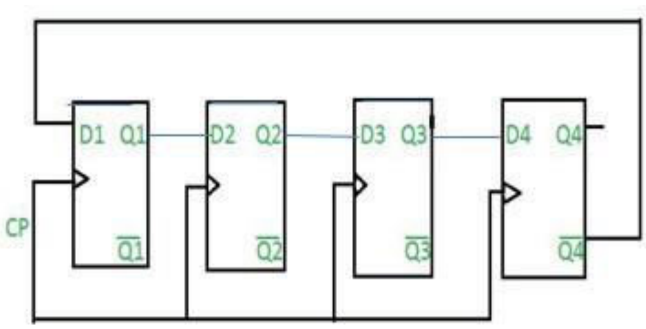

Fig. 3. . Johnson Counter based on TSPC D – flipflops.

TABLE II. TRUTH TABLE OF JHONSON COUNTER

CP	Q1	Q2	Q3	Q4
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0

B. Asynchronous UP Counter

Counters classified as asynchronous have an output that is insensitive to the clock signal. Since the flip flops in asynchronous counters receive different clock signals, the output could be delayed. Only a few logic gates are needed for the relatively simple design of asynchronous counters. "RIPPLE counters" is another name for these counters. A ripple counter's count, such as Mod 2, Mod 4, etc., is determined by how many flip-flops it contains. The total number of output states that the counter can have is denoted by the term "modulus" or "MOD". Up to 2n states can exist in a counter at once, where n is the total number of flip-flops the counter uses. Asynchronous counters have an output that is independent of the clock signal[18-20]. There could be a delay in the output. the generation. As an illustration The maximum number of outputs for a counter with two flip flops is four, Thus, it is referred to as a "Modulus 3 counter" , A particular kind of digital counter that increases its count value with each clock pulse is called an asynchronous up counter. In this case, "asynchronous" refers to the fact that each flip-flop in the counter is activated by the clock signal separately from the others. Every flip-flop sets off the subsequent one in the series [21-22]. The Fig. 4 below shows a 3-bit asynchronous up counter with a data flip flop. It has a counting range of 0 to 9. Each flip flop has a Data input connected to one of the flip flop's state outputs. Additionally, each flip flop has a cascaded clock input. This suggests that Every positive or active edge of the clock signal will cause the flip flops to toggle. The initial flip flop is linked to the clock input. The yb output of the flip flop before It functions as the remaining flip flops in the counter's clock signal input. If there is a positive edge in the clock signal, the initial flip flop's output will change. The asynchronous 3-bit up counter flip flop Due to The flip flops are toggled together, so after one clock pulse, the output will become 20 if the The clock input is linked to the initial flip flop (1).The rising edge of each flip flop's y output activates its clock input, turning on the flip flop after it. It applies an input and sets Half that is the next clock frequency. The individual flip flops y outputs (Q_0, Q_1, Q_2) represent the count of the 3-bit up counter.

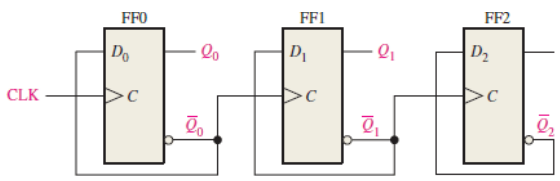

Fig. 4. Asynchrounous UP counter

C. Asynchronous Down Counter

A The 3-bit down counter counts from 9 to 0. Each flip flop has a D input, or data input, linked to logic 1, and each flip flop has a cascading clock input. This suggests that Every active edge, or positive edge, of the clock signal will cause the flip flops to toggle. The initial flip flop is connected to the clock input. The clock signal input is received by the other flip flops in the counter from y rather than from the Yb output of the flip flop that came before it. The three bit down counter's count is shown here by the values Q_A, Q_B, Q_C. When the first flip flop's output changes, the clock signal's positive edge occurs. For instance, the up counter will determine that the next count is two if the current count is three. The next flip-flop's output (count) will change in response to the input clock. The way a down counter operates is completely different from how an up counter operates. The Fig. 5 below shows a 3-bit asynchronous down counter with a data flip flop. The number of each flip flop in this case will decrease with each clock pulse at the input. The down counter therefore starts at 9, 8, 7, and so on. Since asynchronous clock signals are used in the design of both up and down counters, their use is limited due to their unreliability at high clock speeds[23-24].

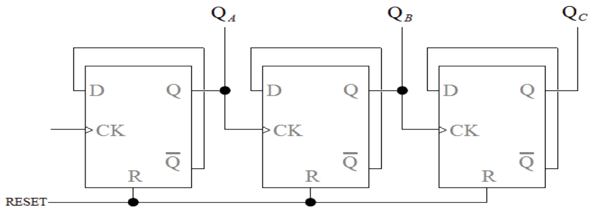

Fig. 5. . Asynchrounous Down counter

III. RESULTS AND DISCUSSION

The work is executed in an organized fashion. The H-spice tool is used to implement the CMOS technology's simulation of the D Flip- Flop. Figure 6 displays the results that were obtained. When the clock is low, feeding the d-flipflop with toggling inputs 1 and 0 generates the result shown in Fig. 6. The result in this instance will be 0. On the other hand, the output and input signal will be identical when the clock is high. The layout and matching simulated outcomes of the FinFET-based D-Flip Flop The experiment's outcomes are displayed in Fig. 6. The output of the d-flipflop when its inputs 1 and 0 are toggled while the clock is low is depicted in the figure. The result in this instance is 0. On the other hand, the output and input signal will be identical when the clock is high. Fig. 7 shows the FinFET-based D-Flip Flop's design and corresponding simulated results. Using this D-Flip Flop (TSPC technique), the design and The corresponding waveform of the TSPC D flip-flop (FinFET) are shown in Figs. 8 and 9, respectively. Johnson Counter (FinFET) results obtained with a 3-bit Johnson counter are shown in Fig. 10. A Johnson counter is an inverted ring created by the output's feedback to its own input. Here, we have 8 usable states (2^3 states) for a 3-bit counter. It was decided to design an asynchronous up-counter and down-counter. The results of the simulation are displayed in Figs. 10, 11, and 12. These values are obtained from a 3-bit synchronous counter with a 7-state count. A counter composed of flip-flops connected serially encounters a clock pulse. Because of the ripple clock pulse, it is frequently identified as a ripple counter. An asynchronous counter may have up to $2^n - 1$ possible counting states. The flip-flops' own inverted outputs are connected to each of their inputs. An up-counter and a down-counter are the same except for the ports that connect to the display. The non-inverted output, y, is connected to the display for up-counters. On the flip side of the hand, the inverted output (Yb) for a down counter is connected to the display.

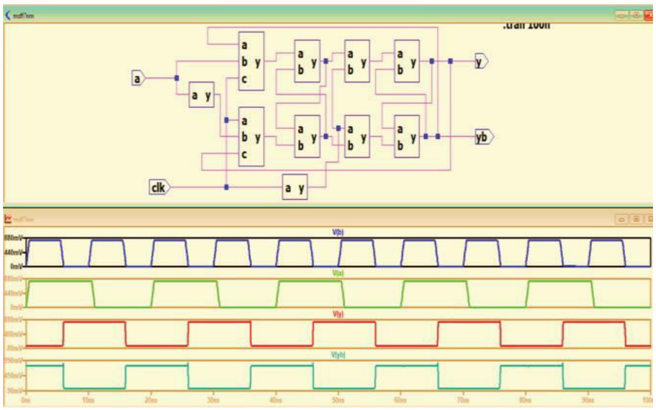

Fig. 6. D flip-flop (CMOS) Circuit and Output Waveforms.

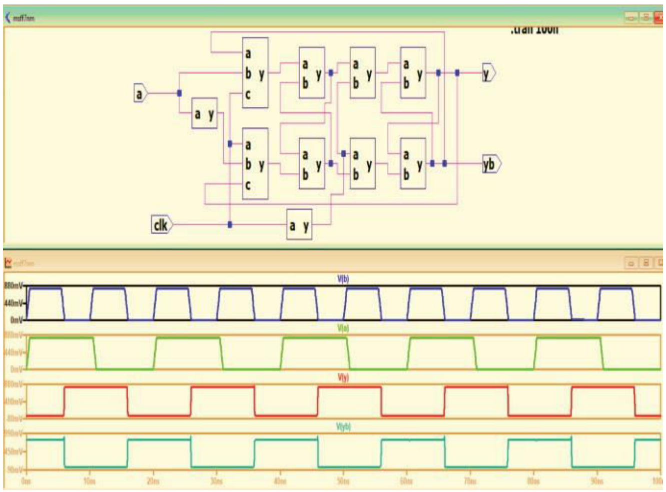

Fig. 7. D flip-flop (FinFET) Circuit and Output Waveforms.

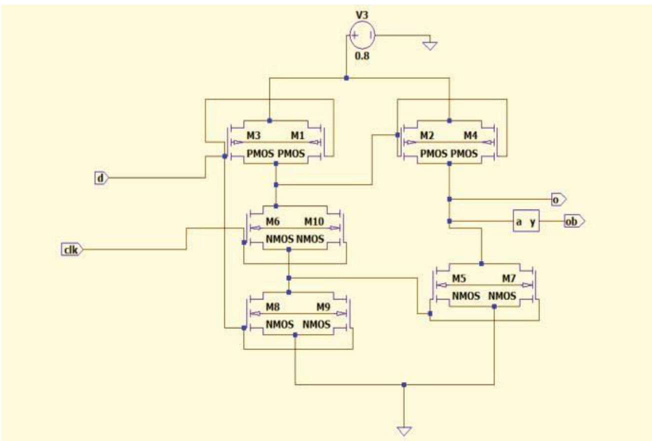

Fig. 8. TSPC D flip-flop (FinFET) Circuit

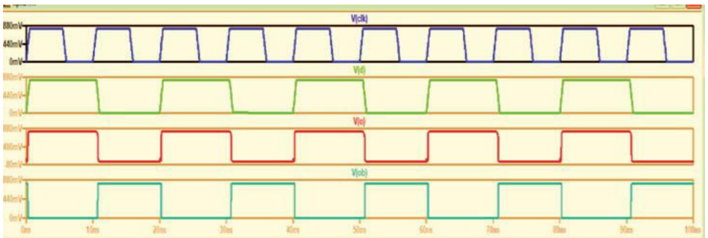

Fig. 9. TSPC D flip-flop (FinFET) output waveforms

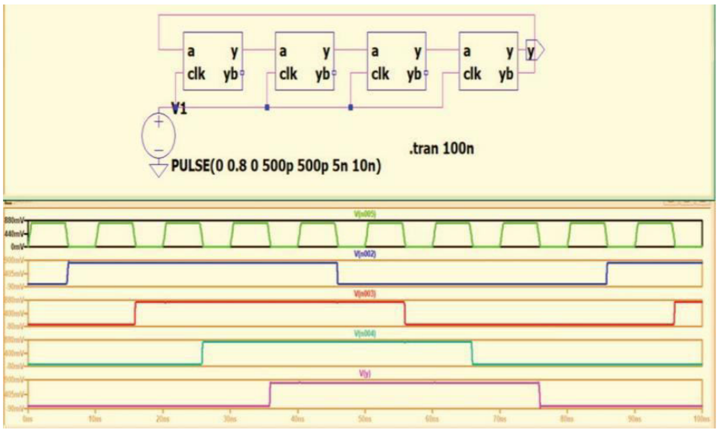

Fig. 10. Johnson Counter (FinFET)

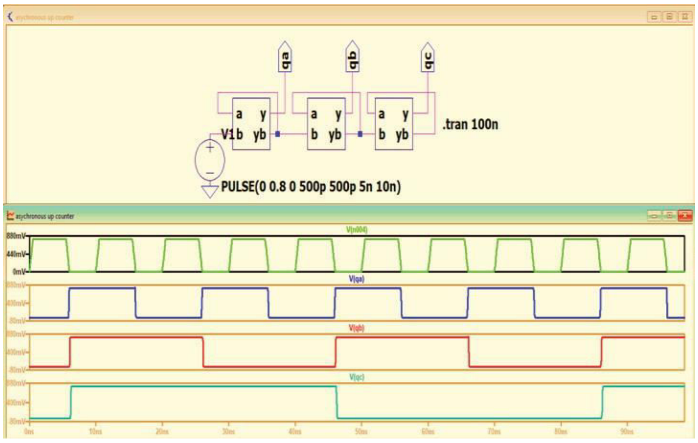

Fig. 11. Asynchronous down-counter

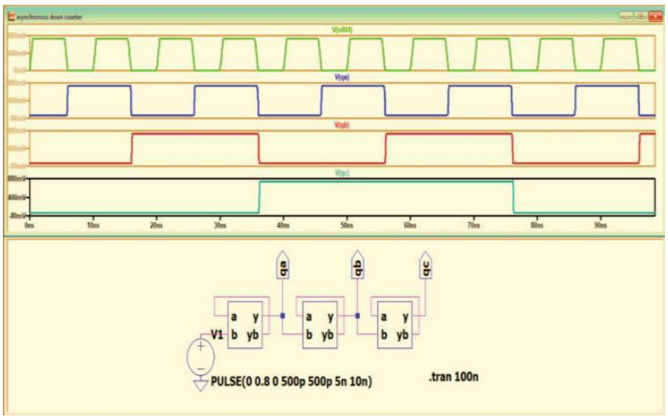

Fig. 12. Asynchronous UP Counter

TABLE III. COMPARISON OF D – FLIP FLOPS

Technology	Operating voltage(v)	Power Consumption(pw)	Noise
CMOS	1	168.05	2.235(v^2/Hz)
FinFET	0.8	50.569	1.071(v^2/Hz)

TABLE IV. COMPARISON OF JOHNSON COUNTER BASED ON TECHNOLOGY

Technology	Operating voltage(v)	Power Consumption(pw)	Noise
CMOS	1	82.46	3.413(v^2/Hz)
FinFET	0.8	35.35	1.842(v^2/Hz)

TABLE V. COMPARISON OF ASYNCHRONOUS COUNTERS BASED ON TECHNOLOGY

Technology	Operating voltage(v)	Power Consumption(pw)
CMOS	1	76.97
FINFET	0.8	55.55

Table .3 shows a comparison of D- Flip flop using CMOS and FinFET technologies. Table .4,5 shows a comparison of Johnson , Asynchronous counters between CMOS and FinFET. From the comparison it can be conclude that the power consumption and noised are much more scaled downed when we are adopting FinFET Technology.

IV. Conclusion

Counters and D Flip-Flop based on Double Gate FinFET 10nm technology using LT-SPICE are implemented. For implementing Counter initially Master -slave flipflop is designed using both conventional CMOS and FinFET Technology then comparison of performances of both technologies is studied in the aspects of average power and noise. To reduce transistor count TSPC technique is used to implement D Flip-Flop in both CMOS and FinFET technology. FinFET shows superior performance than bulk silicon MOSFET and shows notable reductions in area and power consumption. Power consumption and noise are reduced by 57.13%, 46.02% when counter are designed with the help of FinFET based D-Flip Flop. The proposed counters can be implemented in digital signal processing (DSP) for wide range of applications including filters, modulators, and demodulators etc.

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