Design of Low Power Current Steering DAC using 45nm CMOS Technology

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Abstract—Digital to analog converters (DACs) enable the smooth integration of digital technology with analog systems by precisely converting digital signals into analog outputs. This conversion guarantees accurate reproduction of music, video, and other analog signals. A current-steering operates by varying the currents through different branches of a resistor network to produce the desired analog output voltage. The current steering DAC offers energy-efficient applications since it offers a notable reduction in power usage while maintaining accuracy. This work uses a current steering mechanism and Sigma-Delta modulation for 10-bit resolution. The DAC has been designed in
0.45 µm CMOS technology. The precision and stability provided by the integrated Band Gap Reference circuit reduce errors and improve overall dependability. The design includes a segmented structure with 5 bits for binary and 5 bits for unary architecture. In simulation, it is found that the power consumption of the DAC is 2.9147mW. The DAC is designed using 1164 transistors. The DAC is observed to obtain accurate results with a supply voltage of 1.8V. The DAC can be used in modern electronic devices for things like audio processing, communication systems, and signal synthesis.

Keywords—current steering dac, cmos, segmentation, resolution, power consumption

I. Introduction

Modern digital systems entail the transformation of analog signals, such as temperature and pressure, into digital signals for enhanced processing convenience. The efficiency of digital signal processing across various processors underscores its widespread adoption. However, post-processing, there is a necessity to convert the signal back to analog format for real-world presentation. This conversion task is handled by Digital-to-Analog Converters (DACs) [1]. This approach allows for high-speed and high-resolution conversions, making current-steering DACs suitable for applications such as audio processing, communication systems, and signal synthesis in modern electronic devices. The overall architecture of the DAC ensures that the segmentation is carried out before the modulation operations, followed by the digital-to-analog conversion operations. This approach reduces the number of bits per period and improves the performance of the DAC, resulting in benefits like reduced filter size and significant memory savings. The proposed segmented DAC is expected to outperform conventional unsegmented DACs, as demonstrated through experimental results in the article. The current steering DAC can then be designed with a binary or segmented architecture. [2]

In a binary architecture, each bit in the digital input corresponds to a separate switch in the circuitry, allowing for precise control over the output voltage. In contrast, a segmented architecture divides the DAC into several segments, each responsible for generating a portion of the full output range. This approach can simplify the design and reduce power consumption.[3] Operating on the principle of switching current sources, it utilizes binary-weighted current cells to generate analog output voltages. These cells, controlled by digital inputs, direct current either to the output or ground, generating an analog voltage proportional to the sum of the weighted currents. With advanced design parameters like low glitch energy and low distortion, coupled with techniques such as dynamic element matching and error correction, Current Steering DACs achieve exceptional accuracy and bandwidth, making them ideal for demanding applications in communication systems and audio equipment.[4]

II. Related Work

The work [3] primarily affects the dynamic performance of the current-steering DAC due to mismatch-induced nonlinearity. The temporal and amplitude mismatches were successfully improved using the dynamic-element-matching (DEM) technique. A current-steering DAC based on an R-2R ladder and a foreground calibration technique are suggested in the work [4]. Mismatches in the current source and resistor have an impact on this kind of converter. A 500 MSPS 8-bit segmented Current Steering Digital to Analogue Converter (CS-DAC) with superior dynamic and static performance is presented in work [5]. Utilizing 180 nm CMOS technology. The suggested CS-DAC architecture uses 3+5 segmentation to reduce the trade-off between space and performance. This paper [6] takes advantage of the design of a 65-nm CMOS process to create a 14-bit two-channel time-interleaved DAC for communication systems. The nonlinearity in the current summation DAC is to be minimized via a new asymmetric current-tree summation network. In addition, a low-complexity duty-cycle calibration technique and differential clock phase are used. In the work [7] a 6-bit full-binary current-steering DAC that is small, lightweight, and optimized for Wireless Personal Area Network applications using 60GHz. The proposed binary structure decreases power

consumption by realizing a compact DAC by doing away with extra circuits like temperature decoders. In the piece [8], a linear wideband Mixing-DAC architecture is presented. A 65 nm CMOS test-chip with a dual 16 bit 2 GS/s 4 GHz Mixing-DAC, IMD 82 dB up to 1.9 GHz, and output noise -165 dBm/Hz is used to validate the proposed method. The current-steering DAC in this study [9] is intended for use in continuous-time ADCs and has minimal latency and high linearity. It analyses in detail the distortion caused by mismatch, noise, and output-impedance associated with similar unary-weighted current-steering DAC architectures. They have proposed a tri-level DAC architecture based on the research findings that may be used to a continuous-time ADC design and attain 12-bit static linearity. To remove distortion caused by output impedance, the solution combines DAC impedance matching with a recommended compensation method. In order to lessen the impact of several nonlinearity sources resulting from designing routing parasitic in a current steering digital-to-analog converter (DAC), this work [10] provides a switching scheme-based placement approach.

III. Proposed Methodology

A. The Proposed Method

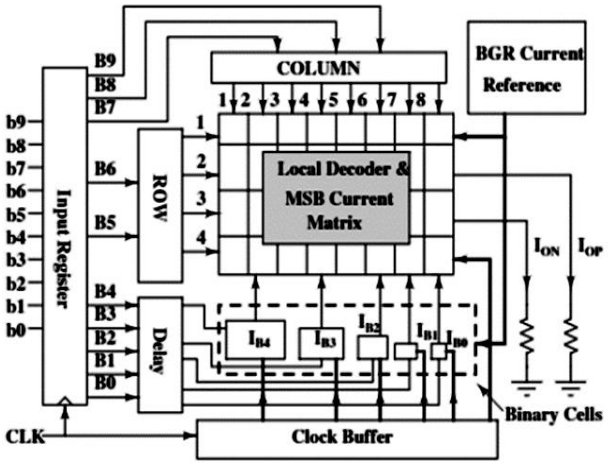

Fig. 1. 10 bits current steering DAC [5]

The proposed method is presented as shown in Fig. 1. 10-bit current steering is a complex electronic device called a digital-to-analog converter is essential for producing accurate analog voltages from digital inputs. The proposed method consists of a register. The register is of 1 bit capacity, it is built using nand gates. 10 registers are cascaded to obtain 10 bits register. The stable input signal from the register is sent to the delay circuit. Segmentation is done as 5 LSBs as unary and 5 MSBs as binary to improve performance efficiency and to reduce area. The unary structure consists of a delay circuit which matches the timing of the signal with the binary architecture. Each current cell has unit reference which I supplied from the Band Gap reference circuit.[11] The binary segmentation involves code conversion from binary to thermometer to reduce glitches. There ae two decoders row and column to reduce area. They are placed in the form of a matrix. The local decoder is used to control the input signals. The BGR circuit provides current source independent of temperature. There are 2 outputs which are positive and negative part of the analog signal respectively. A 10-bit binary input, with each bit denotes a distinct current path that can be opened or closed, is applied to the DAC.

Current steering is the process of controlling a network of MOSFETs organized in a binary tree topology. With the use of the binary tree structure, a vast variety of output voltages can be produced by creating any conceivable combination of currents. A bit that is set to '1' opens the corresponding current path and permits current flow, whereas a bit set to '0' closes the path and prevents current flow.[12] Using the proportional relationship between current and voltage, the total current passing through the output of this DAC determines the output voltage. In order to improve the DAC's linearity, dynamic current calibration is utilised. Each current element's gate must have a reference current stored on a capacitor. In order to account for non-idealities such as charge injection offset, the reference current is shifted via each unit current element throughout a calibration cycle. Because of its dynamic calibration, which guarantees a high level of output voltage precision, for more accuracy.[13]

B. D Input Register

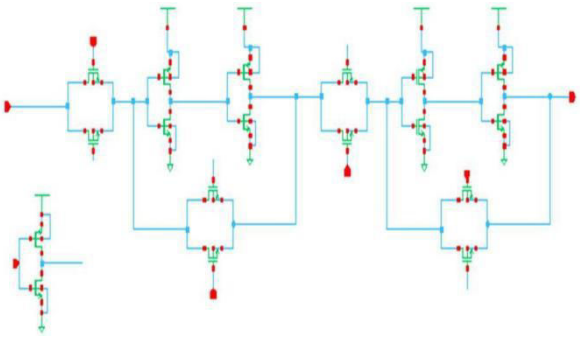

Fig. 2. D Flip Flop

A DAC with 10 bits is the one being examined. Thus, we need a 10 bits input register in order to provide input to the 10 bits converter. The register's main job is to synchronize the digital input data with the circuit clock. The input register is a PIPO (Parallel In Parallel Out) register. PIPO was selected because it allows any number of bits to be switched on in response to a particular digital input. A master-slave positive edge triggered D flip-flop is being used to implement the 10-bit register. Transmission gates and CMOS technology are used in the implementation of the D flip-flop. Fig. 2 shows the D flip-flop's CMOS implementation. The D flip-flop's master stage transmits the D-input to the master stage output without restricting it when the clock pulse value is low. With the aid of the feedback circuit, the slave functions as a holding circuit at this moment, holding the value that was present at the previous clock. The slave stage samples the data from the master stage and the master stage functions as a holding circuit when the clock pulse is rising. The input value immediately preceding the clock's rising edge is the output value. [14]

C. Band Gap Reference Voltage

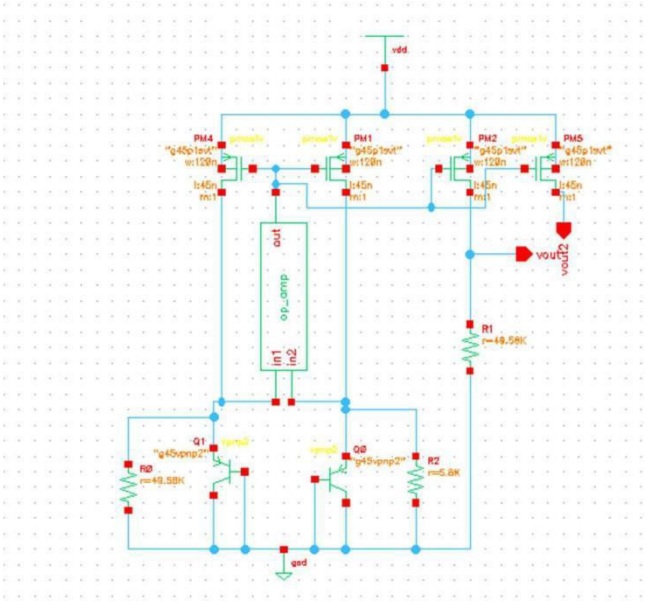

Fig. 3. Band Gap Reference circuit

The BGR circuit is another essential part of integrated circuits as shown in the fig 3. In analog and mixed-signal systems, this circuit is crucial for supplying a steady and precise voltage reference that guarantees consistent performance regardless of changes in supply voltage and temperature. The bandgap voltage phenomena in semiconductors, where the difference in energy between the valence and conduction bands stays constant across temperature, is used by the BGR circuit.[15] The BGR circuit makes use of a voltage divider to generate a portion of the supply voltage with the use of properties that vary with temperature. The components such as diodes with temperature-dependent characteristics produce currents that are proportionate to the absolute temperature (PTAT). These PTAT currents are then replicated using current mirrors, and when they are combined with the voltage divider, which produces a voltage that compensates for temperature-dependent voltage drop. [16] The produced voltage is compared to a reference value using an operational amplifier, and the error signal that results is utilized to modify the circuit to keep the output voltage steady. The drain current is given by the following equation (1). W/L ratio is given by equation (2). By making use of the below relations for drain current, we can calculate W/L ratios for all the transistors.

$$Id = [(Un * Cox/2)(w/l)\,(Vgs - V\,t)\text{^}2\,] \quad (1)$$

$$W/L = [(gm)\text{^}2/((Un * Cox) - Id)] \quad (2)$$

where,

- Id: Drain current
- Cox: Oxide capacitance per unit area
- W: Gate width
- L: Gate length
- Vt: Threshold voltage
- Vgs: Gate to source voltage

D. Row and Column Decoders

Row and column decoders are essential parts of memory organization, especially in memory arrays such as Random Access Memory (RAM). These decoders address particular rows and columns according to supplied addresses, enabling effective memory access. To enable focused data retrieval or storage, the row decoder chooses a certain row, while the column decoder further specifies the column. By activating rows and columns selectively, this addressing system improves memory access efficiency, lowers power consumption, and speeds up access times. Because row and column decoders are scalable and flexible enough to meet the increasing demands of current memory design, they are essential components for higher memory densities and storage capacities.[17]

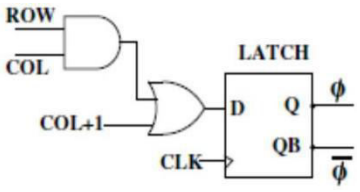

Fig. 4. Local Decoder [8]

Fig.4. illustrates that the final control signal for the control switches is produced by combining the output of the row and column decoders in a local decoder matrix. There are five unary MSB bits in the suggested steering DAC, so that 32 current sources are needed to convert the data. The local decoder matrix will produce 32 control signals, which the control switches need in order to control these 32 current sources. As seen in the image, the local decoder logic for MSB bits is an AND-OR combination. The control signal for the switches will be Q and Q bar value when the AND-OR gate output is coupled to a D-latch.[18] Row and column decoders contribute to faster memory access times. By directly addressing the specific row and column, the time required to locate and retrieve data is minimized. Row and column decoders provide flexibility in memory organization. Memory arrays can be designed with various configurations, and the decoders allow for the implementation of different addressing schemes. Decoders contribute to reduced power consumption by enabling the selective activation of rows and columns. Unnecessary activation of entire arrays is avoided, leading to more energy-efficient memory access operations.[19] The precision of the 10-bit DAC, stability of the BGR current reference circuit, and efficiency of row and column decoders collectively contribute to the seamless operation of integrated circuits in various electronic applications.[20]

E. Source Matrix

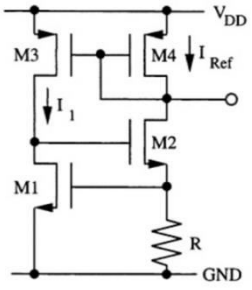

Fig. 5. Current mirror circuit [6]

Five unary and five binary architectures make up the proposed 10-bit DAC. As can be seen in Fig.5, the binary architecture requires current sources that are binary weighted. "N" current sources are needed for every N bit of conversion. The number of sources needed for n conversions is equal to (2n - 1) in the situation of unary architecture, where all current sources used are of the same value. For binary architecture, we went with LSB bits since they needed a binary weighted value.[21] The unary architecture receives the MSB bits. Making ensuring the unary current sources are binary weighted in relation to the binary source value is one thing to be sure of. For 5 unary bits, there are currently 32 sources available. In order to feed the row and column decoder signals to the sources appropriately, they are formatted in a matrix. It also needs three different kinds of sources. The value of the LSB source is 5uA. The following LSB source has a value of 10uA, whereas the unary-structured MSB source has a value of 20uA.[22]

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

The simulations are executed in cadence using gpdk45 nm technology. Each component is design using appropriate instances and by giving correct properties The following results are obtained which are as follows.

A. D flip flop

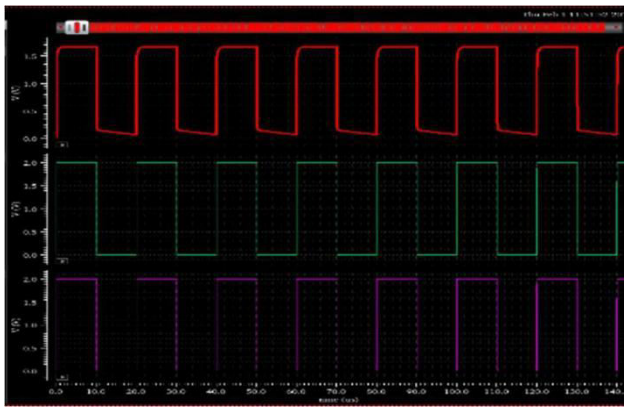

Fig. 6. D flip flop transient analysis

The D flipflop is used to obtain stable signal. It is observed that the output of flipflop is found to be 1v as shown in Fig.6. with respect to the input which is also 1v.

B. Operational Amplifier

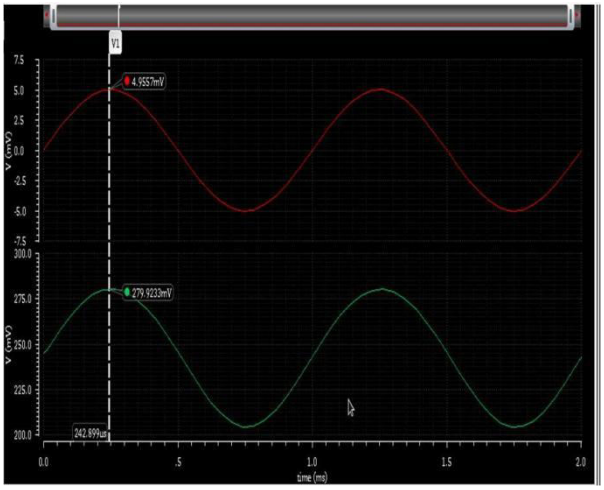

Fig. 7. Op amp transient analysis

With the Op amp set to high gain, a bandgap reference can be built. A single stage OPAMP may provide a gain of about 35–40 dB. However, gains of up to 60 dB can be achieved by employing a two-stage OPAMP. [23] The output signal of the Op amp is found to be amplified by 200 times the input which is shown in Fig.7.

C. DAC structure

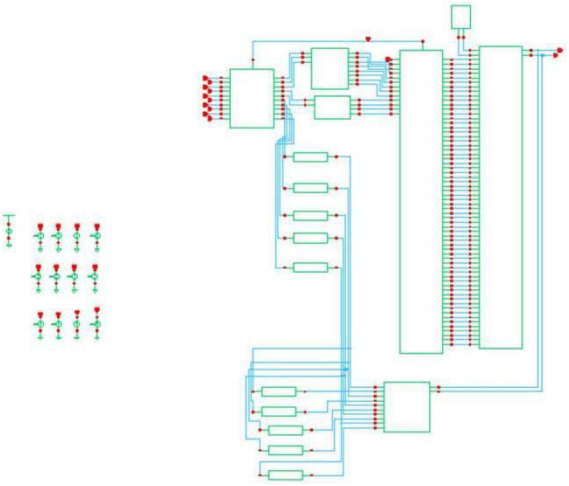

Fig. 8. Schematic of Steering DAC

The schematic of current steering DAC is as shown in Fig 8. It consists of register, row decoder, column decoder, buffer circuit, inverter, local decoder matrix, switch and source circuit and BGR circuit all cascaded together.

D. DAC Output Waveform

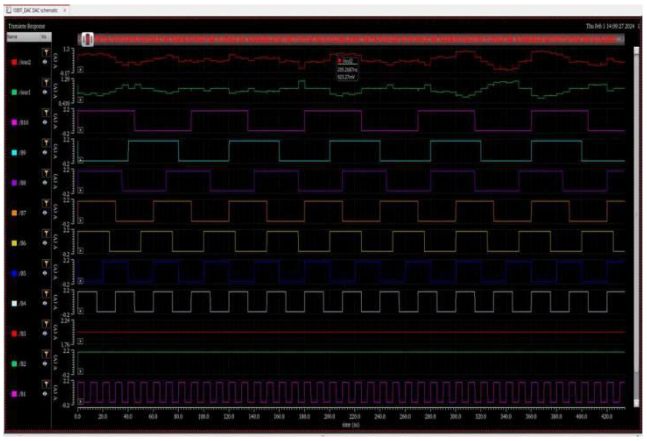

Fig. 9. DAC transient Analysis

The Fig. 9. shows that the output waveform of the DAC represents the positive and the negative part of the analog signal. The analog output can be verified using the formula given by,

$$Vout = (Vref/2n - 1) * Digital\ input \quad (3)$$

where,

- Vout : Output Voltage
- Vref : Reference Voltage
- n: Resolution of DAC

TABLE I. SHOWS THE COMPARISON OF PROPOSED WORK WITH THE EXISTING WORKS

Reference no.	Power consumption (mW)	Resolution (bits)	Area	CMOS Technology (nM)	Power Supply (V)
Proposed Work	2.9147	10	1164 transistors	45	1.8
[1]	11.07	12	0.25 pVS	180	1.8
[5]	11.07mW	8	-	180	1.8
[7]	17.7mW	6	0.038mM^2	90	1.2
[8]	380mW	16	1.6mM^2	65	2

Table.1 shows the comparison between previously existing works and the proposed work. It is observed that the power consumption of the proposed work is significantly less which is about 2.91mW. From the obtained results, the design of current steering DAC using segmented architecture illustrates accurate analog conversions with low power consumption. However this DAC uses a supply voltage of 1.8V which implies that for a supply a of less than 1.8 V, the results may vary. The DNL plot suggests that the DAC is not free of errors resulting in lesser accuracy. This limitation can be acknowledged by using Current Mode Logic Latch (CML). For any system design, there is always trade-off between parameters. Based on the application in which the DAC is used, necessary parameter is improved.

V. CONCLUSION

The 10-bit segmented Digital-to-Analog Converter (DAC) in this work has been proposed as a current steering DAC using 45nm CMOS technology. To attain the desired performance, the DAC combines segmented architecture. Compared to earlier research, this steered digital audio coder guarantees less glitches. Since fewer transistors are used in the design of the various components, the DAC's power consumption is greatly decreased. Thus, in contemporary electronic equipment, it is appropriate for uses like signal synthesis, communication systems, and audio processing. The specifications, including the necessary resolution, speed, power consumption, and cost, have a significant impact on how a segmented DAC is designed. In comparison to previous works, the suggested work exhibits a significant increase in performance. However, there are few limitations regarding conversion speed and accuracy which can be rectified using CML latch and differential switches.

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