"Design of a Low-Glitch Double-Edge Triggered Flip-Flop for Low-Power VLSI Systems"

S. Kiran [1], S.Salma [2], T.G. Tejaswini [3]

[1]PG Scholar, [2]Assistant Professor,[3]Assistant Professor, Dept of ECE, Anantha Lakshmi institute of technology & sciences, Anantapuramu

Abstract - Dual edge triggered (DET) methodology is the most popular preference for the research workers in the field of VLSI designing due to its low power consumption and high-performance quality. DET methods provide the same throughput at half of the clock frequency in comparison with the single edge triggered (SET) methods. This can lessen the half power consumption and commit to total system power savings. In this paper, a low power glitch free advanced dual edge triggered flip flop (DETFF) design is proposed. The proposed novel DETFF is constructed by using the combination of C-element circuit and 1P-2N structure. If any error affects one of the structure, then it is nullified by the other one structure. To limit the input burdening, the two circuits are combined to contribute the transistors connected to the input. This DETFF has used an internal dual feedback structure. The presented DETFF reduces the area and average power consumption and gain the higher speed of the system. Analysis of the temperature impact on power and delay at different supply voltages has also been done. Novel DETFF is implemented with 22nm CMOS technology.

Keywords: Clock distribution network; Dual edge triggered; Glitches; Power consumption; Power delay product.

I. INTRODUCTION

Presently, in VLSI designing, the flip-flops are widely used for information storage. Device's performance and fault tolerance capability are precisely affected by the flip flop's speed, power consumption and reliability. Consequently, this is essential to design the flip-flops for minimum power consumption, propagation delay, area and maximum reliability with highest fault tolerance capability. The latest studies have shown that in digital VLSI designs, device scaling minimize the supply voltage and device capacitances and circuit becomes more sensitive to the glitches. When particles touch the drain side of a MOSFET, electron hole combinations take place. The opposite biased electric field induce a drift transient current [1-2].

The voltage transient as a result of the collected charge is named a transient fault. In memory circuits, transient faults may be formed by the prior combinational circuit glitches. Low power consumption may be achieved efficiently by supply voltage scaling. Power consumption because of the glitches cannot be neglected as the portion of total power consumption varies from 9% to 38% [3]. Presently, in integrated designs, the designing of energy efficient circuits is one of the hard challenge for the research workers [4]. In [5-6], the authors presented latch configurations which have reduced the average power consumption and also reduced power delay product (PDP).

The clock distribution network may consume about 45% of the total system power [7]. Clock network consumes more power, therefore, this is required to minimize the total number of clocks. To minimize the number of clocks, the true single phase clock (TSPC) approach has been advised with the basic registers [8]. To minimize the clock power consumption, the frequency of the clock can be scaled down, by sampling the input data on both of the rising and falling edges of the clock, without modify the system throughput. The DET approach minimizes the half power consumption of the clock network system. Although DET circuits have extra complexity in comparison with the SET circuits however this can be more energy efficient [9].

In this paper, the existing designs are reviewed in part II. The presented novel glitch free DET-FF design is discussed in part III. The results and analysis are discussed in section IV and conclusions are given in section V.

II. EXISTING DET-FF DESIGNS

Dual edge triggered flip flop provides the equivalent data rate like single edge triggered flip flop at the 50% of the clock frequency, that can minimize the power consumption logic designs [10-11]. Bonetti et al. [12] presented a dual edge triggered flip flop, as shown in Fig. 1, to overcome the built in clock overlap challenge, by using TSPC circuits instead of an inverted clock and make clear the point of clock overlapping by using the TSPC circuits and an internal two-fold feedback design. The Dual Data Rate Flip Flop (DDR-FF) that has a reduced clock load because of its easy structure, reduced activity factor and its hard edge quality factor [13]. Devarapalli et al. [13] proposed a robust LM_C DET-FF by using C-elements, where the straight clock pulses used to latch the data for the minimize of clock dynamic power consumption without any other pulse generator structure. This flip flop configuration gives the additional robust solution for dual data rate (DDR) flip flops due to absence of complications in it with less transistor count.

Fig. 2 shows the LG_C configuration that upgraded with common latch MUX dual edge triggered flip flops, because of this fact, flip flops internal node data never changes with the changes in the input. The LG_C configuration presented improvement in the energy dissipation [14]. The glitch resistant LG_C dual edge triggered flip flop designed by three C-element circuits, which are two internal latches and one output latch, with the inverting topology because of the transistor level implementations.

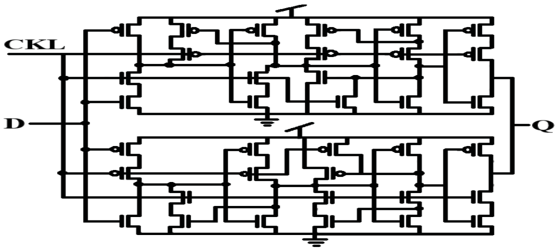

Fig. 1. TSPC-DET-FF.

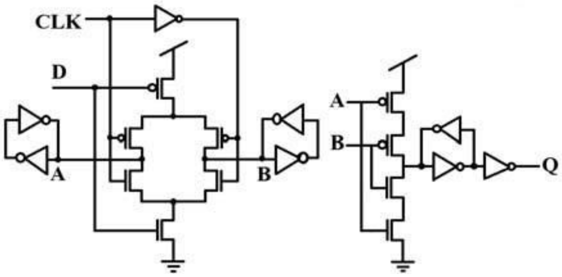

Fig. 2. LG_C-DET-FF.

Fig. 3 shows the low power glitch resistant dual edge triggered flip flop design (D1-DET-FF) which minimizes the power consumption and delay and expand the efficiency and speed of the system [15]. The design is constructed by using the combination of C-element structure and 2P-1N circuit. In D1-DET-FF configuration, if any glitch changes the data of one structure then it is nullified by the other one structure. To limit the input burdening, the two structures are combined to share the transistors connected to the input. In this design an internal two-fold feedback circuit is used [15].

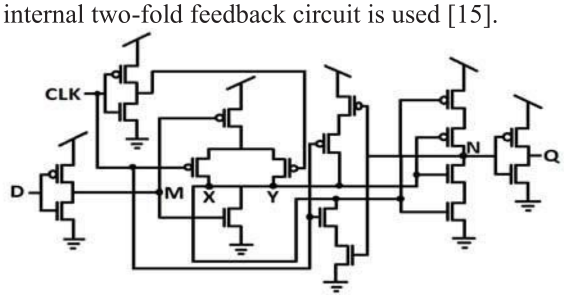

Fig. 3. D1-DET-FF.

To reduce the switching activity, in most cases, the C-element circuits [16] are used. The C-element design has the different aspect that when it's both inputs are equivalent, thereupon output switches to its input values; when the inputs are not equivalent, thereupon its output goes to the high impedance situation it means output will be in its past situation. The 1P-2N circuit [17] is different from the C-element structure: 1) When the inputs are not equivalent then the output may not go to the high impedance situation. 2) The C-element circuit has four transistors, but 1P-2N structure has three transistors only.

III. NOVEL GLITCH FREE DET-FF

Currently, the main motive of the research workers is to get small area, low power and high speed in VLSI designing. Consequently, so many techniques have been considered by the research workers in VLSI applications. We have designed a glitch free advanced DET-FF design, shown in Fig. 4.

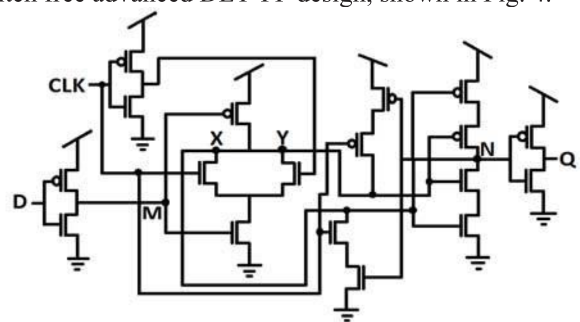

Fig. 4. Proposed design with 1P-2N structure and C-element circuit.

Existing DET-FF designs [12, 14] are constructed by using the C-element circuits only. The presented glitch free DET-FF is a novel robust low power glitch free design and designed by the mixed combination of 1P-2N and C-element circuits that can work accurately at low voltage supply. It provides the totally glitch free output that can improve the system efficiency. The presented model consumes less power and provides glitch free output. The working procedure of this design is as follows: I, the glitch either filter out or propagate to the output Q. II, if glitch propagates to the output Q, then it is filtered out through the feedback path. Here, we just clarify how this design can avoid the glitches that can occur at the input node D from the prior combinational designs.

Now we can assume that the initial state of nodes M and N to be M=0, N=0, X=1, Y=1, the output Q=1 and clock **clk=0**. At the node M, if any error or glitch exist from the prior combinational design, then the value of the node M will be changed from 0 to 1. For the first 1P-2N structure, the input combination becomes M=1 and clk=0. For this input combination, first 1P-2N structure's output goes to the high impedance condition, consequently, its output remains in its prior condition that is X=1. For the second 1P-2N structure, the inputs are M=1 and clk=1, so for this input combination, second 1P-2N structures output Y=0. Now for the C-element circuit, the inputs are X=1 and Y=0, therefore, its output goes to the high impedance condition meaning that its output remains in its past condition that is N=0, so the output becomes Q=1. Therefore, we can look that there is no difference in the output state.

Now considering nodes M and N to be M=1, N=1, X=0, Y=0, the output Q=0 and **clk=0**. If any fault occurs at the node M, then the node value will be altered from 1 to 0. For the first 1P-2N structure, the inputs are M=0 and clk=0, consequently, the first 1P-2N structures output is X=1. For the second 1P-2N structure, the inputs are M=0 and clk=1, therefore, second 1P-2N structures output is Y=1. Like now for the C-element structure, the inputs are X=1 and Y=1, then the C-element structures output switch to its input values that is N=1, therefore the output becomes Q=0, repeatedly we can look that there is no difference in the output state.

Now considering nodes M and N to be M=0, N=0, X=1, Y=1, the output Q=1 and clock **clk=1**. At the node M, if any error or glitch occurs from the prior combinational circuit, then the node value will be altered from 0 to 1. For the first 1P-2N structure, the inputs are M=1 and clk=1. For this input combination, first 1P-2N structures output is X=0. For the second 1P-2N structure, the input combination becomes M=1 and clk=0, for this input combination, second 1P-2N structures output go to the high impedance condition, so, its output is in its prior state that is Y=1. Now for the C-element circuit, the inputs are X=0 and Y=1, so, its output go to the high impedance condition it means output is in its prior condition that is N=0, so the output becomes Q=1. So, we can look that there is no difference in the output condition.

Now considering nodes M and N to be M=1, N=1, X=0, Y=0, the output Q=0 and **clk=1**. If any fault occurs at the node M, then the node value will be altered from 1 to 0. For the first 1P-2N structure, the inputs are M=0 and clk=1, for this input combination, first 1P-2N structures output is X=1. For the second 1P-2N structure, the inputs are M=0 and clk=0, therefore, second 1P-2N structures output is Y=1. Like now for the C-element structure, the input combination becomes X=1 and Y=1, then the C-element structures output switch to its input values that is N=1, therefore the output becomes Q=0, again we can look that there is no difference in the output condition. Thus, the incorrect input data is left out without any changes in area, power and time. Thus, the proposed design is completely glitch-resistant and have high-speed and high-efficiency.

IV. RESULT AND ANALYSIS

The proposed DET-FF design is performed through the SPICE simulator with Predictive Technology Model (PTM) 22 nm CMOS technology [18] at a power supply of 1V.

TABLE I. RESULT ANALYSIS OF DIFFERENT DET-FFs				
DET-FFs	***TSPC [12]***	***LG_C [14]***	***D1-DET-FF [15]***	***Proposed Design***
$P_{avg. cons.}$ (µw)	7.825	8.988	3.049	3.011
$t_{p(D-Q)}$ (ps)	65.536	84.297	26.995	26.165
$t_{p(CLK-Q)}$ (ps)	43.213	63.281	25.896	25.013
PDP (fJ)	0.513	0.758	0.082	0.079
No. of transistors	38	28	18	18

The channel lengths for the transistors are taken to 22 nm. In the latest technologies, the operating voltage decreases and the frequency increases. Therefore, we have taken 1V operating voltage and frequency fixed to 500 MHz's. Although the operating frequency is large enough, then the output will not reduce. The performance evaluation results are reported in Table 1. The average power consumption, power delay product and propagation delay comparisons are indicated in table and calculated and verified for existing DET-FF designs. We note that the proposed DET-FF design has a small number of transistors, the lowest power consumption, the lowest power delay product (PDP) and the lowest delay in comparison with existing designs, as shown in Fig. 5.

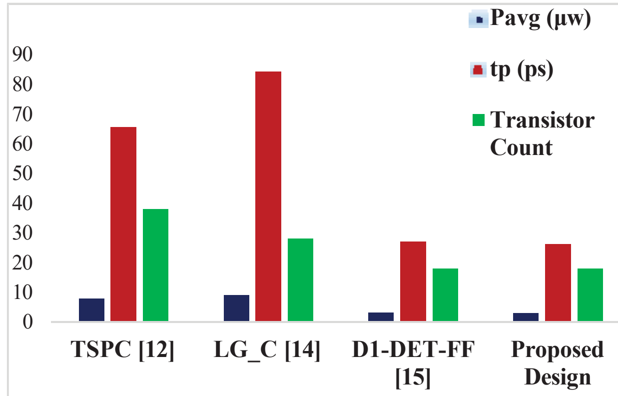

Fig. 5. Power, delay and area comparisons of different DET-FFs.

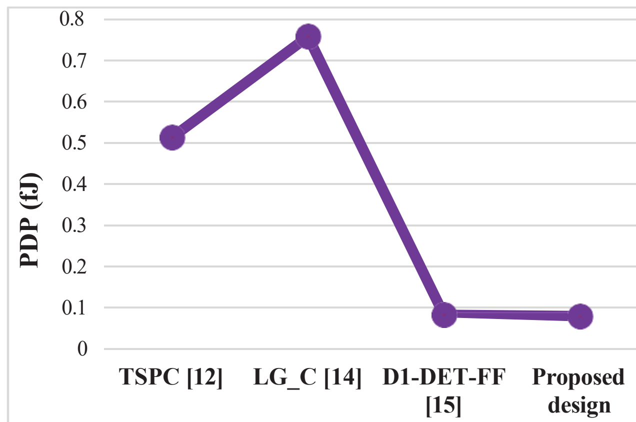

Fig. 6. PDP comparison of different DET-FFs.

Consequently, the proposed design has high efficiency as compared to existing dual edge triggered flip flop designs. The power delay product analysis is shown in Fig. 6, which shows that the resented design has the lowest power delay product. Due to the lower delay and lower average power consumption, the proposed designs have lower PDP. The propagation delay analysis of proposed DET-FF with temperature variations at different supply voltages is presented in Table 2. The delay rises with the temperature rises but decreases with the supply voltage increment. Temperature affects the carrier mobility and the threshold voltage (V_t). When the temperature increases, both the carrier mobility and the threshold voltage decrease, consequently, the timing performance of a circuit design depends on the supply voltages.

TABLE II. PROPAGATION DELAY ANALYSIS OF PROPOSED DET-FF

Temperature (^{0}C)\Power supply	*0.7V*	*0.8V*	*0.9V*	*1V*	*1.1V*	*1.2V*
-60	47.712	42.347	31.275	21.916	16.961	14.056
-40	52.458	45.389	32.984	22.181	17.489	15.922
-20	57.649	50.264	35.697	22.998	18.071	16.018
0	70.076	58.206	40.927	23.986	19.918	17.028
20	89.185	68.541	45.622	25.365	22.695	19.998
40	105.93	79.95	67.025	41.475	38.085	33.505
60	120.89	97.95	79.986	67.675	61.298	50.245
80	149.02	129.23	109.04	89.902	75.304	61.042

Due to the temperature increment, obviously decrement in threshold voltage results in an increment of both the propagation delay and the output transition time, although decrement in the carrier mobility produces completely different variation of the timing performance.

and the frequency rises, therefore, delay rises with the frequency rises. Due to the supply voltage minimization, power consumption reduces but propagation delay rises. Due to the delay rises, the average power consumption also rises with the frequency increment, as indicated in Fig. 8.

TABLE III. AVERAGE POWER CONSUMPTION ANALYSIS OF PROPOSED DET-FF

Temperature (^{0}C)\Power supply	*0.7V*	*0.8V*	*0.9V*	*1V*	*1.1V*	*1.2V*
-60	1.568	2.133	2.372	2.537	2.885	3.205
-40	2.027	2.228	2.553	2.751	2.994	3.533
-20	2.203	2.456	2.876	2.998	3.316	3.912
0	2.388	2.631	2.989	3.001	3.687	4.198
20	2.422	2.795	3.001	3.003	4.003	4.538
40	3.698	3.958	5.001	5.479	6.502	7.415
60	4.695	5.546	7.011	7.524	8.855	9.705
80	6.054	7.987	9.047	9.978	11.387	12.223

TABLE IV. AVERAGE POWER CONSUMPTION ANALYSIS OF PROPOSED DET-FF AT HIGHER V_T.

Temperature (^{0}C)\Power supply	*0.7V*	*0.8V*	*0.9V*	*1V*	*1.1V*	*1.2V*
-60	1.001	1.233	1.781	2.037	2.335	2.685
-40	1.127	1.388	2.001	2.251	2.594	3.023
-20	1.308	1.686	2.188	2.381	3.002	3.465
0	1.658	2.031	2.534	2.698	3.117	3.798
20	1.981	2.392	2.739	2.898	3.497	4.128
40	2.308	3.058	3.692	3.976	4.582	5.415
60	3.197	4.016	5.001	5.524	6.125	6.895
80	4.154	5.089	5.987	6.564	7.468	8.213

Due to the technology scaling, the leakage current increases and also increase the total power consumption. To reduce the total power consumption, one possible solution is to use higher threshold voltage. Average power consumption analysis of proposed DET-FF with temperature variations at higher V_t at different supply voltages is presented in Table 4. The Average power consumption reduced by using the higher threshold voltage. Fig. 7 shows the delay analysis of proposed DET-FF with frequency. The propagation delay rises with the frequency variations (from 25MHz - 1000MHz). To minimize the delay, we have to increase power supply voltage but in latest technology (22nm) the power supply voltage minimizes

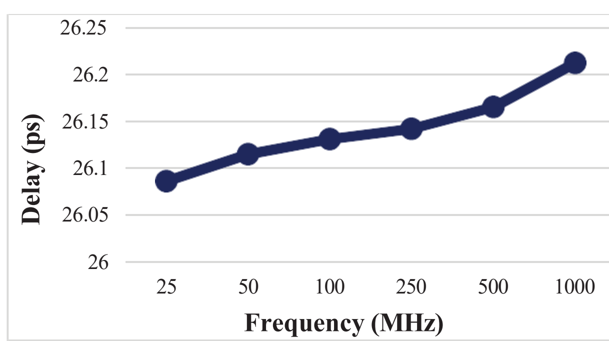

Fig. 7. Propagation delay analysis of novel DET-FF with different frequencies.

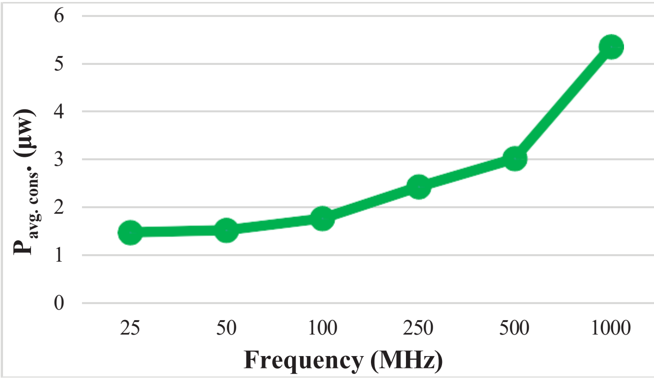

Fig. 8. Average power consumption analysis of novel DET-FF with different frequencies.

V. CONCLUSION

A glitch free DET-FF with the mixed combination of 1P-2N structure and C-element circuit has been proposed. The proposed design is constructed by using two fault resistant structures. For comparison between novel design and existing designs we have taken 1V power supply voltage and clock frequency of 500 MHz and the proposed design implemented with 22 nm CMOS technology and simulated through the SPICE. If any error or glitch affects one of the structure, then it is nullified by the another structure. This design provides the totally glitch resistant output and can improve the system efficiency. The novel design can decrease the half power consumption and commit to the total system power savings. Due to the implementation of this design with fault resistant structures and an internal dual-feedback structure, obtain robust and static operation. The proposed design has the lowest average power consumption and lowest PDP in comparison with the existing DET-FF designs. The proposed DET-FF has the less transistor count, consequently, occupies less area and has the small delay, therefore, provides the high speed and high efficiency. We also analyzed the temperature impact on power and delay. The power consumption and delay increase with the temperature increment. Higher threshold voltage has been used to reduce the power consumption.

REFERENCES

[1] C. M. Hsieh, P.C Murley, and R.R. O'Brien, "Collection of charge from alpha-particle tracks in silicon devices", IEEE Trans. Electron Devices, vol. 30, no. 6, pp. 686–693, June 1983.

[2] R.C. Baumann, "Soft errors in advanced semiconductor devices: Part I: The three radiation sources", IEEE Trans. Device Mater. Rel., vol. 1, no. 1, pp. 17–22, March 2001.

[3] L. Benini, M. Favalli, and B. Ricco, "Analysis of hazard contribution to power consumption in CMOS IC's", Proceedings of the International Workshop on Low Power Design, pp. 27-32, 1994.

[4] R.G. Dreslinski, M. Wieckowski, D. Blaauw, D. Sylvester, and T. Mudge, "Near-threshold computing: reclaiming Moore's law through energy efficient integrated circuits", Proceedings of the IEEE, vol. 98, pp. 253-266, Feb 2010.

[5] Sumitra Singar and P. K. Ghosh, "Fault-Free D-Latch Configurations for Low Power Applications", Journal of Nanoelectronics and Optoelectronics, ISSN/ISBN: 1555-1318, vol. 13, no. 5, pp. 701-707, May 2018.

[6] Sumitra Singar and P. K. Ghosh, "Unique Robust Fault Resistant D-Latch for Low Power Applications" in International Conference on Computer, Communications and Electronics (Comptelix), ISSN/ISBN: 978-1-5090-4708-6, pp. 16-20, 978-1-5090-4708-6/17/$31.00 ©2017 IEEE, July 2017.

[7] H. Kawaguchi, and T. Sakurai, "A reduced clock-swing flip-flop (RCSFF) for 63% power reduction", IEEE JSSC, vol. 33, pp. 807-811, May 1998.

[8] Y. Yuan, and C. Svensson, "High-speed CMOS circuit technique", IEEE Journal of Solid-State Circuits, Vol.-24 (1), pp. 62-70, Jan 1989.

[9] M. Alioto, E. Consoli, and G. Palumbo, "DET FF topologies: A detailed investigation in the energy-delay-area domain", IEEE ISCAS, Rio de Janeiro, Brazil, pp. 563-566, July 2011.

[10] N. Nedovic, and V.G. Oklobdzija, "Dual-edge triggered storage elements and clocking strategy for low-power systems", IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 5, pp. 577–590, May 2005.

[11] A.G.M. Strollo, E. Napoli, and C. Cimino, "Analysis of power dissipation in double edge-triggered flip-flops", IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 8, no. 5, pp. 624–629, May 2000.

[12] A. Bonetti, A. Teman, and A. Burg, "An overlap-contention free true-single- phase clock dual-edge-triggered flip-flop", Proc. IEEE Int. Symp. Circuits Syst., (ISCAS), pp. 1850–1853, 2015.

[13] S.V. Devarapalli, P. Zarkesh-Ha, and S.C. Suddarth, "A robust and low power dual data rate (DDR) flip-flop using c-elements", 11th Int'l Symposium on Quality Electronic Design, IEEE, 978-1-4244-6455-5/10, pp. 147-150, April 2010.

[14] S. Lapshev, and S.M.R. Hasan, "New low glitch and low power DET flip-flops using multiple c-elements" IEEE Transactions on Circuits and Systems, DOI-10.1109/TCSI.2016.2587282, vol. 63, no. 10, pp. 1673-1681, Oct 2016.

[15] Sumitra Singar, N. K. Joshi and P. K. Ghosh, "A Glitch Free Novel DET-FF in 22nm CMOS for Low Power Application", Journal of Nanotechnology, Hindawi, ISSN/ISBN: 1687-9503, vol. 2018, Article ID 2934268, 10.1155/2018/2934268, pp. 1-6, March 2018.

[16] D.E. Muller, "Theory of asynchronous circuits", Internal Rep. no. 66, Digit. Comput. Lab., Univ. Illinois at Urbana-Champaign, 1955.

[17] A.K. Pudi N S, and M.S. Baghini, "Robust Soft Error Tolerant CMOS Latch Configurations", IEEE transactions on computers, vol. 65, no. 9, pp. 2820-2834, Sept 2016.

[18] Berkeley predictive technology model, [Online] Available: http:/ www. ptm.asu.edu/~ PTM, Accessed 2018.