A Design of Low Power and High Speed Encoder and Decoder Circuits by Re-Evaluating High Speed Design Values

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Abstract: Nowadays, the rapid improvement in CMOS technology to reduce power and area and to increase the speed of chip is mainly consideredin research field.In this paper power dissipation and delay are reduced using Transmission Gate Logic(TGL), which are the most challenging factor in CMOS VLSI Design.The power reduction is achieved without compromising the performance. It is difficult to design such devices because tradeoff between power consumption and speed is a major concern. The encoders and decoders in this paper are designed using proposed TGL by which trade off problems can be eliminated to a greater extend.The number of transistors reducedis four in AND Gate.In OR Gate the power is reduced more than half even with two transistors increased in proposed design.The circuits are designed using 45nm technology in CADENCE VIRTUOSO and the performance parameters are analyzed.

Key Words: Transmission Gate, Encoder, decoder, AND Gate, OR Gate.

I. INTRODUCTION

The improvement in VLSI technology lets us to fabricate the chips which contains millions of transistors.So,nowadays the need forlow power VLSI technologyclaims to be high. The different design levels of VLSI technologies are circuit, architectural,layout and the process technology level. By selecting a good logic style for implementing logic circuits the circuit level design has become considerable power savings[1].

CMOS Integrated Circuits is presently being used as it dissipates less power than the bipolar junction transistor. By the use of transmission gate the power consumed by the circuit will be less as compared to CMOS logic.Thus instead of using traditional CMOS pull-up and pull-down networks,transmission Gate Logiccan be used to construct logic circuits[2].

In this paper, we are going to study about the performance of encoder and decoder based on speed and power in transmission gate logic in 45nm technology by using cadence software.

A. Transmission Gate

Transmission Gate is a parallel combination of PMOS transistor and NMOS transistor. Both PMOS and NMOS transistors work simultaneously.Over the entire input voltage range TG provides a low resistance path between input and output terminals[3].The TG selectively passes the input signal to the output based on the voltage given to the gate input.

The NMOS transistor has three or four terminals. In three terminal NMOS transistor gate, drain, source is the terminals where as in four terminal NMOS substrate is the additional terminal. The NMOS transistor is built with n-type source, n-type drain and p-substrate. Electrons are carriers in NMOS transistor. On applying high voltage as the gate input, the NMOS will be in ON condition but on applying low voltage as the gate input, the NMOS will be in OFF condition. Since electron speed is twice as fast as holes, NMOS transistor is faster than PMOS transistor. The NMOS IC will be smaller than PMOS ICs. It provides one half of the impedance as that of PMOS transistor. The NMOS transistor operates by forming an inversion layer in a p-type transistor substrate. Applying voltage to the gate terminal, n-channel is created.

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Fig 1 shows the symbol of a transmission gate

with input and output terminals and the controlling gate terminal.

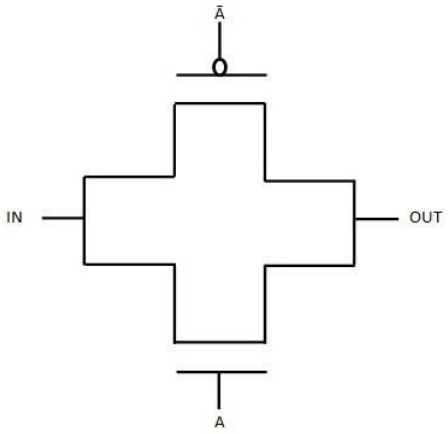

Fig 1.Symbol of Transmission gate.

B. Encoder

An encoder is combinational circuit that converts all its input data one by one at a given time into one encoded output[4]. A binary encoder is a many input circuit that process logic "1" data at input into its equal binary code at output[5]. In general anencoder consists of 2^N input signals and N output signals. Fig 2 shows the block diagram of aencoder. The outputs of the encoder are based on the Boolean functions. Each output line has its own Boolean function according to which the output is obtained.

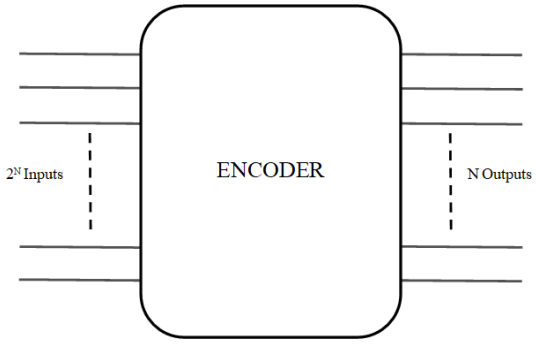

Fig 2. Block diagram of Encoder.

C. Decoder

Decoder is a combinational circuit that consists of many input and output signals. In a decoder the inputs are given as coded signals and processed in the decoder to obtain a different set of coded output signals. The output shows all the details about the input signals given at the decoder input. A decoder is designed using AND gates only which leads the outputs to be in active high condition. A decoder is a logic circuit which reverses the encoder operation, the original information can be obtained by decrypting the encodedvalue[6]. It is a digital circuit consisting of N inputs and 2N outputs[7]. Fig 3 shows the general representation of the decoder.

The combinational block is designed based on the speed and power[8]. Decoders are widely used in memory system of computers, where they respond to the address code input from the central processer to activate the memory storage location specified by address code.

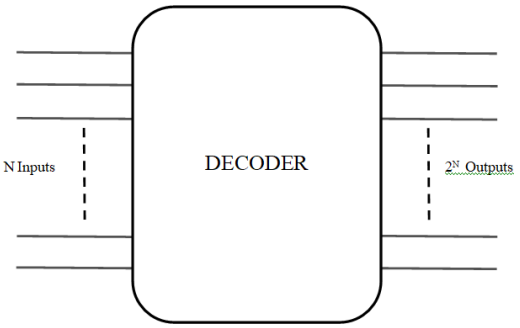

Fig 3. Block diagram of Decoder.

II. EXISTING SYSTEM

Here, the AND and OR Gates are constructed using TGL .In AND gate,the circuit is designed using Transmission Gates whichconsists of inverted inputs. Two inverters are used for inputs at the gate terminal of the transistors[9]. In this design the AND operation is done with the help of two transmission gates which consists of two PMOS and two NMOS transistors. The inverted inputs are given as gate inputs to both PMOS transistors in Transmission Gate.

The OR gate is designed using two Transmission Gates. The gates oftwo NMOS transistors and one PMOS transistor are connected to the same input line. There is no need for inverted inputs in OR gate[10].

In the existing AND Gate totally there are eight transistors used. In the existing OR Gate totally there are four transistors used in the design.

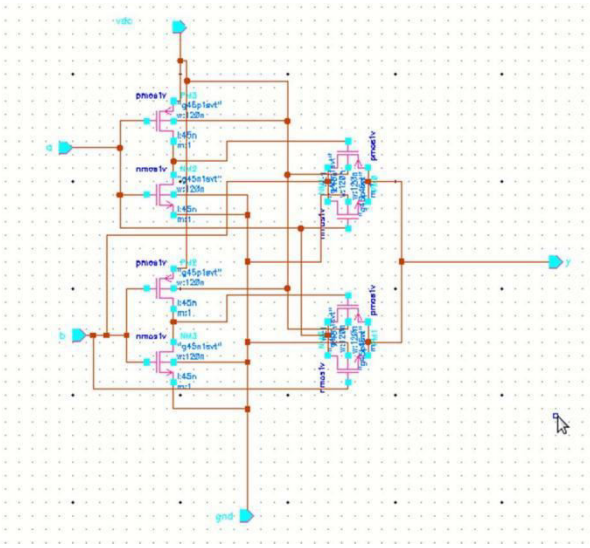

Fig 4. Circuit of AND Gate using TGL.

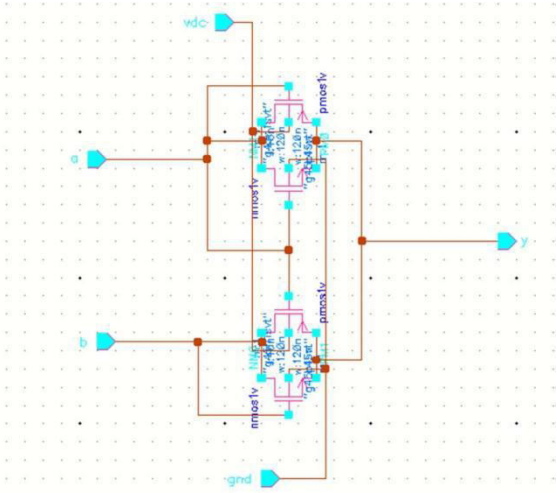

Fig 5. Circuit of OR Gate using TGL.

III. PROPOSED SYSTEM

In proposed method the static power, dynamic power, power dissipation is reduced using TGL.

The static power is the power used even when the circuit is in idle state. It is due to the sub threshold conduction through the idle transistors, tunnel current through gate oxide. Complementary MOS transistor has static power consumption whereas transmission gate have negligible static power. The dynamic power is the power wasted when the circuit is under working condition. Capacitive load charging and the current occurring during switching are the two components that promote dynamic power consumption. Transmission gate has lower dynamic power consumption compared to CMOS transistor. Power Dissipation is resolute by the amount of energy needed to charge and discharge the load capacitance at desired switching frequency. Power dissipation of digital circuit comprises of static power and dynamic power. Power dissipation is more crucial in battery driven applications. Power dissipation normally leads to heat generation in the device that is eliminated by the use of heat sink. A sink has a thermal resistance which is lower than the device. So it draws heat from the device. For the effective heat reduction, heat transfer rate from the area of heat generation to the ambient must be greater than the heat generation rate. Our work deals with reduction of power dissipation using TG which eliminates the need for heat sink.

The AND Gate is designed without using the inverting inputs. Thus the number of transistors is reduced to fourwhich leads to decrease in power dissipation occurring in circuit and increased the operating speed of the AND Gate.Fig 6 shows the circuit design of proposed AND Gate.

Though there is one inverter present at the input terminal of the OR gate the power dissipation is very less when compared with the existing system. By using strong '1' weak'0' concept in the proposed design the power dissipation is reduced drastically.Fig 7 shows the circuit design of proposed OR Gate.

In the proposed AND Gate totally there are four transistors used. In the proposed OR Gate totally there are six transistors used in the design.

The 4:2Encoderand 8:3 Encoder are designed by using proposed OR Gate. The 2:4 Decoder and 3:8 decoder are designed using proposed AND Gate.

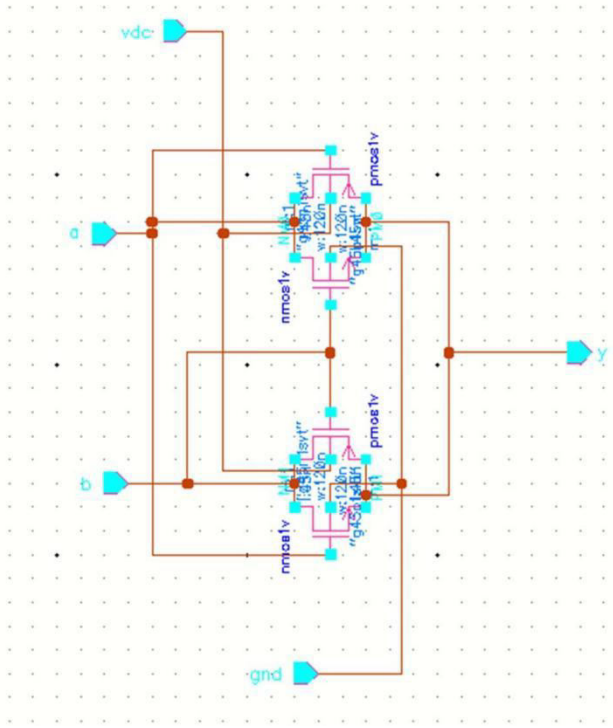

Fig 6. Circuit of Proposed AND Gate.

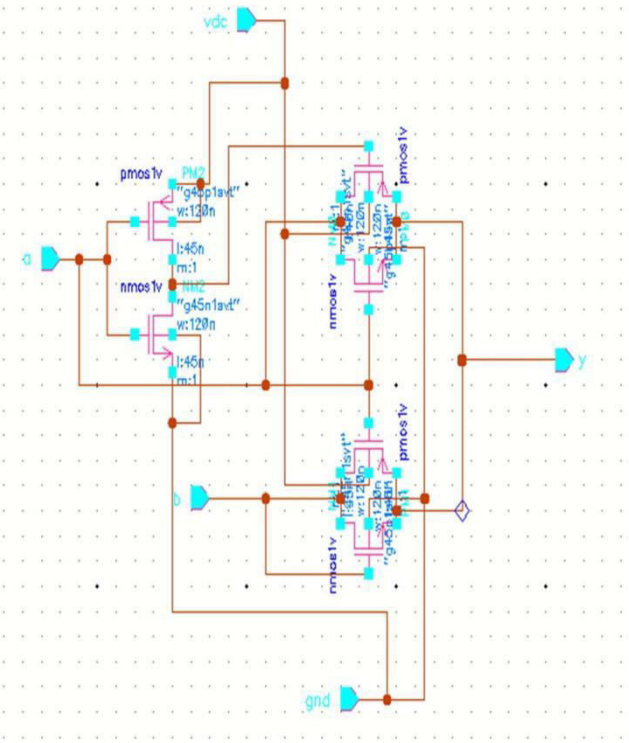

Fig 7. Circuit of Proposed OR Gate.

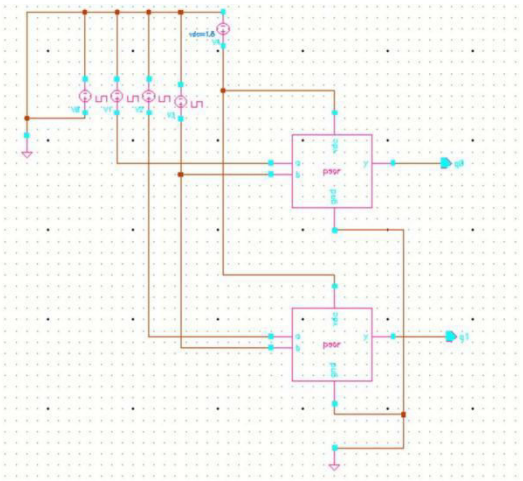

Fig 8. Circuit of Proposed 4:2 Encoder.

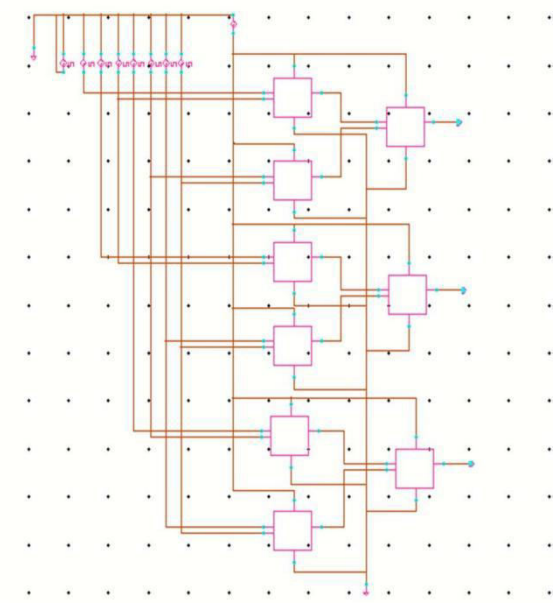

Fig 9. Circuit of Proposed 8:3 Encoder.

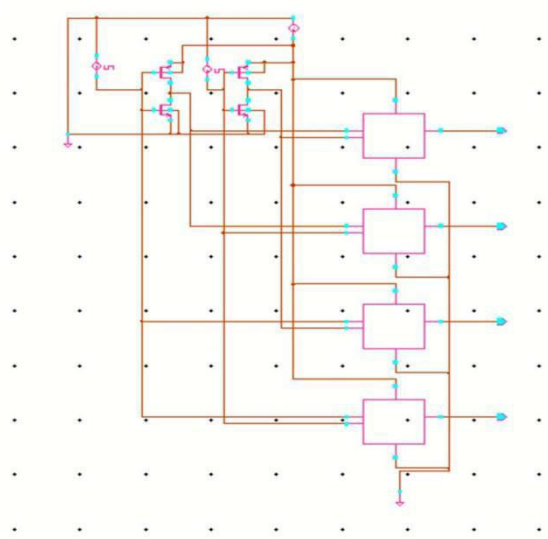

Fig 10. Circuit of Proposed 2:4 Decoder.

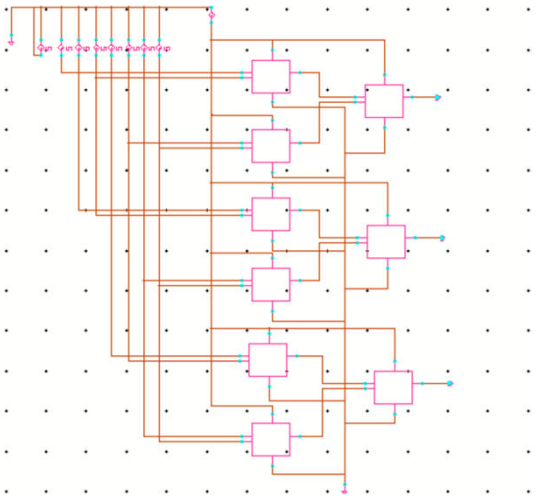

Fig 11. Circuit of Proposed 3:8 Decoder.

IV. RESULTS AND DISCUSSION

The transient analysis is done for all the logic circuits in 45 nm technology using CADENCE VIRTUOSO. The power and delay is calculated with help of the output waveform. In the existing design the power value is in terms of micro watts (µW) and the delayvalue is in terms of nano seconds (ns). In the proposed design the power value is in terms of nanowatts(nW) and the delay value is in terms of pico seconds(ps). The minimum power obtained in the proposed designs is 4.027nW and the minimum delay in the proposed design is 1.010ps.

Table 1 depicts the power difference in existing and proposed values. Table 2 shows the delay values inexisting and proposed designs.

TABLE 1: POWER ANALYSIS OF LOGIC CIRCUITS

LOGIC CIRCUITS	EXISTING VALUES (µW)	PROPOSED VALUES (nW)
OR GATE	24.760	16.250
4:2 ENCODER	99.000	66.550
8:3 ENCODER	150.400	102.000
AND GATE	0.043	4.027
2:4 DECODER	40.740	118.500
3:8 DECODER	64.120	305.800

TABLE 2: TIME(DELAY) ANALYSIS OF LOGIC CIRCUITS

LOGIC CIRCUITS	EXISTING VALUES (ns)	PROPOSED VALUES (ps)
OR GATE	3.775	3.263
4:2 ENCODER	10.010	4.631
8:3 ENCODER	39.370	13.510
AND GATE	10.000	1.010
2:4 DECODER	15.320	7.763
3:8 DECODER	28.170	12.490

The output waveform of various logic circuits are shown below.

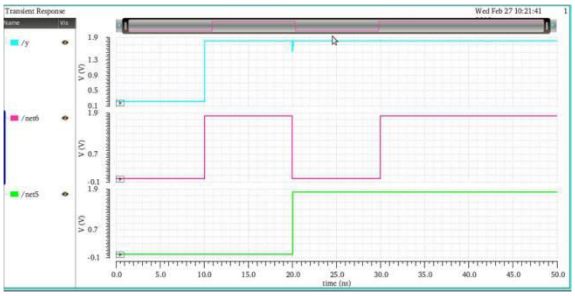

Fig 12. Output wave of Proposed ORGate.

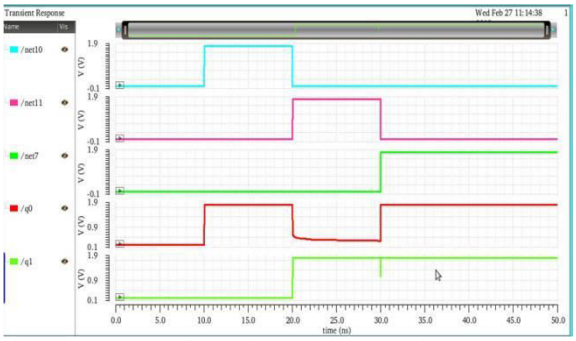

Fig 13. Output wave shape of Proposed 4:2 Encoder.

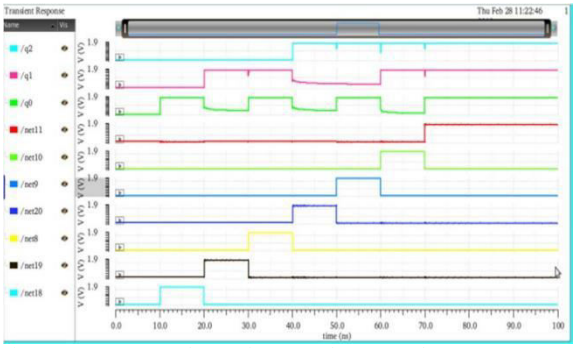

Fig 14. Output wave shape of Proposed 8:3 Encoder.

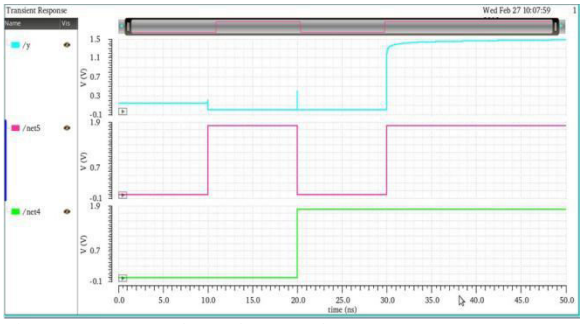

Fig 15. Output waveform of Proposed AND Gate.

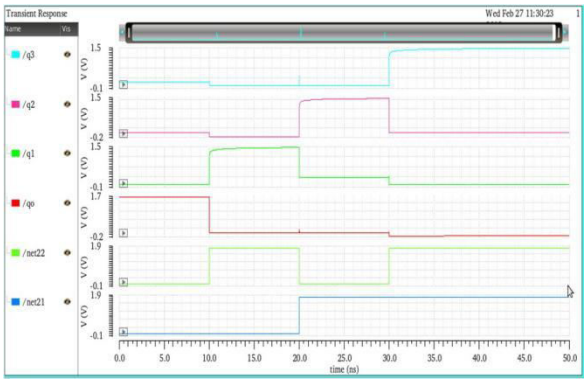

Fig 16. Output waveform of Proposed 2:4 Decoder.

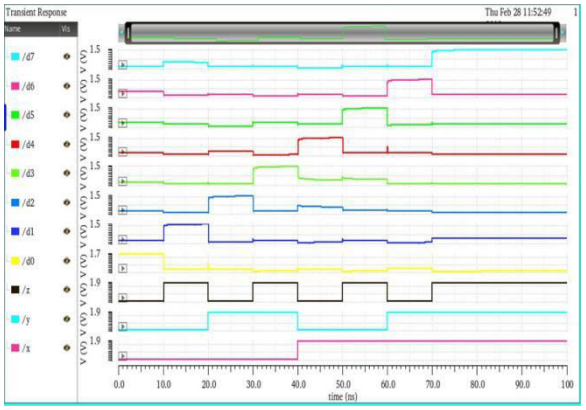

Fig 17. Output waveform of Proposed 3:8 Decoder.

V. CONCLUSION

In this paper we have studied about Encoders and Decoders that are designed using transmission gate with V_{dd} (1.8V) as supply voltage. Circuits are designed and simulated at 45 nm technology. The bidirectional element (i.e.transmission gate) used here is considered to be the fast switching element than the CMOS transistor. The simulation results and the analysis shows that the power and delay is reduced in the proposed design.

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