

## “Design of a Hybrid Multiplier-Based Optimized MAC Unit”

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*Abstract—* Wherever there is a need for high-performance computing applications there is an evident demand of an efficient high-speed multiplier. Multiplication takes most significant time as compared to other arithmetic operations. Multipliers are the most essential blocks in every high-performance computing architecture like Digital signal processing (DSP). MAC unit which consist of Multiplier and Accumulator plays an important role to decide the performance of any DSP block. The better performance of MAC unit fulfills the parameter of fast computation and real-time processing capabilities of a DSP. Over the years number of ideas have been proposed to improve the performance and mitigate the excessive partial product term generation during conventional multiplication approach. In this paper, we have focused on proposing the MAC architecture using an integrated Hybrid binary Multiplier and integrated CLA adder network. The integrated multiplier is a combination of Karatsuba algorithm and Urdhva Triyagbhyam sutra from vedic mathematics. CLA adder network consist of CLA and conditional sum adder which helps to reduce addition time by performing parallel addition. Mentioned design is implemented in Verilog HDL using Libero SOC PolarFire v2.1 tool, targeting its PolarFire FPGA family and MPF300T\_ES-1FCG484E device.

*Keywords—* DSP; MAC unit; Karatsuba multiplication algorithm; Urdhva Triyagbhyam Sutra; CLA; Verilog HDL; FPGA

### I. INTRODUCTION

The Multiplication and accumulation (MAC) operation is the main computational block in Digital Signal Processing (DSP) architecture. This block decides the overall performance of the architecture as it has significant & dominating execution time. Designing high speed MAC is the demand for real time DSP applications those covers the application area like Machine vision, Avionics (Radar), defence, audio signal processing. To reduce the computation time, power consumption and complexity of circuit the Analog signal processing is being performed in digital domain with the help of various DSP algorithms like DFT, FFT. These algorithms have two basic operations i.e. multiplication and accumulation. By reducing the partial product generation during multiplication improves the speed of the MAC. In this paper, we introduce the MAC unit architecture implemented using runtime reconfigurable hybrid binary multiplier design. Since multiplication consumes the significant execution time of the MAC unit there is a need of high speed multiplication algorithm that can compensate/mitigate this significant contribution of multiplication step. Excessive partial product generation in a higher bit multiplication limits the performance of a multiplier. We have implemented the

multiplication with the combination of ancient Vedic mathematics and Karatsuba algorithm. Multipliers implemented with vedic mathematics helps to reduce the computational complexity of DSP applications like FFT, DFT, MAC unit with less number of partial product generation during multiplication. Vedic mathematics was rejuvenated from the Vedas which are ancient scripture of Indian culture. Vedic is a Sanskrit word emerged from Sanskrit language which means the collection of information. Swami Bharati Krishna Tirthaji Maharaja gave main sixteen sutras as his dedication to Vedic mathematics after eight years of rigorous research. The conventional method of multiplication involves the approach of multiplying two binary numbers by multiplying each bit of multiplier with each bit of multiplicand and finally sums the all partial product. This approach is associated with the complexity level of  $O(n^2)$  for multiplication of two n-bit numbers and  $O(n)$  for addition [2].

### II. RELATED WORK

Various architecture of multiplier is proposed using the different vedic sutras in literatures [2] [5] [6] [7]. C. Eyupoglu [4] implemented the multiplication using Karatsuba algorithm. The analysis is made done for various bit lengths. Examination parameters for the implemented design were chosen, the number of multiplications and the time taken for multiplication. Other literatures can be also found which gave an extensive study and implementation results of different kind of efficient fast adder network [18] [19]. Monisha Yuvraj et. al. [16] proposed a novel multiplier design which integrates all major sutras of vedic mathematics. Multiplier is designed integrating all these sutras and designed logically multiplexed in such a way that makes it capable of deciding which multiplier block is to be used for optimum results based on the nature of input. Used vedic scaling techniques extends the application up to 64 bits operations. The literature also tabulates the implementation results and compares the results with conventional multiplier and accumulator unit. Li Husn [17] suggested MAC unit architecture using radix-4 Booth algorithm which results into reduced complexity and minimal switching activity that ensures a low power design.

The integration of proper multiplication schemes along with an efficient fast adder network can results an optimized MAC unit architecture. The proposed architecture is motivated from the demand of this integration to improve the performance of MAC unit.

III. VEDIC MATHEMATICS

Vedic mathematics has its origin from ancient Indian scriptures “Vedas”. Vedas itself means “knowledge”. Jagadguru Shri Bharathi Krishna Tirthaji was the first Indian mathematician who gave recognition to all Sutras (formulas) described in our Vedas by publishing his sighting in “Vedic Mathematics Book by Tirthaji Maharaj”. Vedic mathematics is a compilation of sixteen different Sutras to solve complex mathematical problems in a tricky manner within short period of time. Vedic multiplier proposed in this paper is based on Urdhva Triyagbhyam Sutra and Karatsuba multiplication algorithm. In which we employed a hybrid combination of both the algorithm to achieve an optimal solution for multiplication of the lower as well higher number of bits. Following two subsections.

A. Urdhva Triyagbhyam sutra

Urdhva Triyagbhyam is a Sanskrit word that signifies “vertically and crosswise”. We analysis that as the number of bits in multiplication increased there is an area and delay penalty with conventional and Booth multiplier. To encounter this penalty, we use Urdhva Triyagbhyam Sutra which results in less number of partial product generation and less number of hardware demand, hence increased speed and improved area [3].

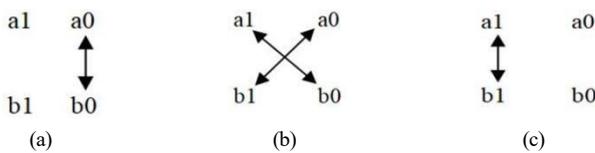
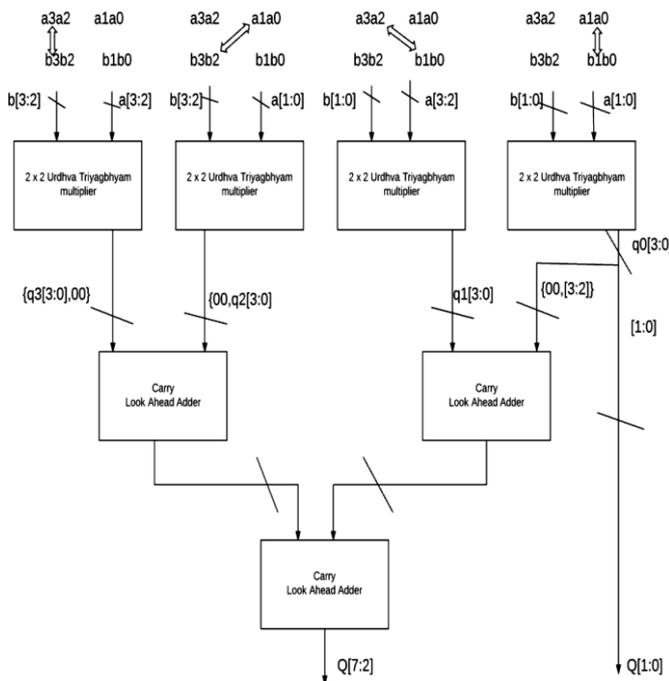


Fig. 1. (a) first step (b) second step (c) third step involved to multiply two 2-bit numbers using Urdhva Triyagbhyam Sutra.



To implement the same logic for a higher number of bits, separate 2x2 multiplier block can be used as explained in fig.

B.Karatsuba Algorithm

Anatoly Karatsuba was the first Russian mathematician who discovered Karatsuba algorithm in 1960 which got publication later in 1962. Karatsuba algorithm gives best results for higher number of bit multiplication. It is based on divide and conquer approach which results in a complexity level of  $O(n^{\log_3})$  multiplication term for two n-bit numbers [4].

The logic behind the Karatsuba Algorithm is to break (divide) the higher number of bits multiplication term into two equal subparts and converting the multiplication term into addition and subtraction operation that helps to reduce the complexity of multiplication which is then converted into addition and subtraction.

Addition is always faster than the multiplication operation consequently the speed of multiplication operation gets increase. Karatsuba algorithm gives best results when there is an input of more than 16 bits and less efficient for less than 16 bits input due to recursion overhead [4].

The interpretation of Karatsuba algorithm for n-bit binary

input A & B: -

Input =  
 $(nOutput=Product)$   
 $(2n-bit)$

B. Carry Look Ahead Adder Network

During MAC implementation, we used CLA Adder network that makes addition much faster since it reduces the carry propagation delay by calculating the carry signal in advance on the basis of input signal provided. The total gate delay for a 4-bit CLA is four which includes two gate delays to calculate carry signal, one gate delay, one gate delay to calculate the propagate and generate signals and one gate delay to calculate the sum signals. Power consumption of the CLA might be slightly higher but the ease of scaling higher bit adders, the lower area and the lesser delay make this trade-

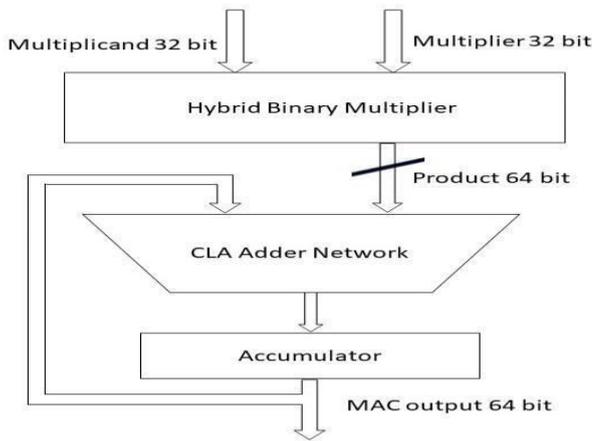


Fig. 3. Architecture of a conventional Multiplier Accumulator unit.

off very slight [15]. We implemented conditional sum adder, using CLA adder. This makes the addition to perform parallel. In conditional sum adder, two sets of output are generated in parallel for given inputs. One set calculates the results by considering the carry input 0 and another set calculates the same considering the carry input 1. Once the correct value of carry is evaluated then it just selects the

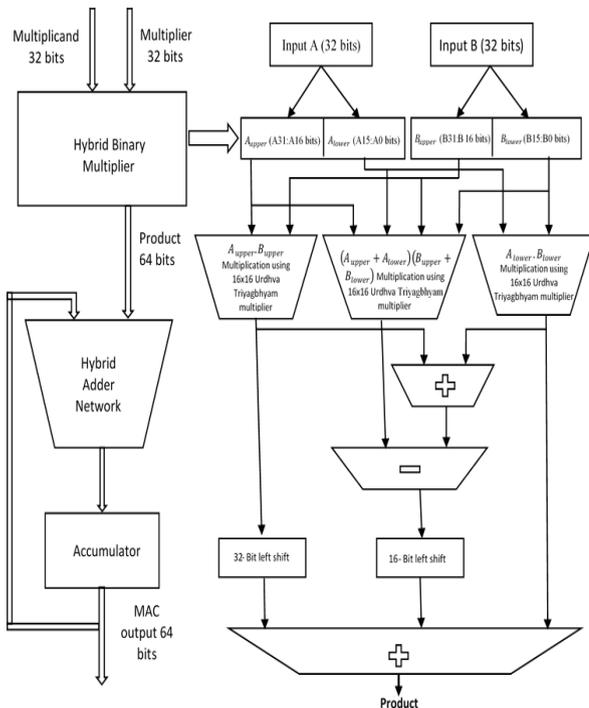


Fig. 4. Proposed MAC unit architecture

correct set of outputs out of two without waiting for the carry signal to ripple through n-bit positions.

C. MAC Unit

Due to advent use of computers and microprocessors analog signal processing is being performed in digital domain with the help of various DSP algorithms like DFT, FFT as the digital domain is less prone to error and more tends to accuracy. These algorithms have two basic operations i.e. multiplication and accumulation. By reducing the partial product generation during multiplication improves the speed of the MAC. A conventional MAC unit consists of a multiplier and an accumulator block along with adder network, the output from the multiplier as added to the value saved in accumulator with the help of adder network.  $AB+C$  is the function which is implemented in a conventional multiplier and accumulator unit.

IV. PROPOSED DESIGN

The proposed MAC unit comprises of a through hybrid multiplier which integrates the advantages of vedic Urdhva Triyagbhyam Sutra and Karatsuba Algorithm combinedly and provides optimum results.

Vedic Urdhva Triyagbhyam Sutra helps in reduction of the generation of large number of partial product significantly, hence multiplication speeds up. But here in Urdhva Triyagbhyam Sutra for binary multiplication, partial products are needed to be added in a ripple fashion that results into increased delay which still makes it unsuitable when we need to perform higher bit multiplication. Karatsuba algorithm gives best result by splitting the higher number of bits multiplication term into two equal subparts and converting the additional multiplication term into addition and subtraction operation. So, our design combines both the algorithm to get optimal performance of the 32-bit multiplier; which takes Urdhva Triyagbhyam Sutra for multiplication of up to 16 bits and Karatsuba Algorithm for the multiplication beyond 16 bits. Implemented adder network also consist of the hybrid CLA and conditional sum adder network. Which helps to speed up the addition by parallel processing. Implemented MAC unit uses the advantages of hybrid multiplier and adder network improving the performance by reduction in the delay. This helps to implement a fast and low power application in DSP block.

V. RESULTS

The proposed design is realized in Verilog HDL using Micosemi's Libero SOC PolarFire v2.1 targeting its PolarFire family with device MPF300T\_ES-1FCG484E. The tools used for simulation and synthesis are Modelsim\_Pro 10.5c and Synplify Pro L-2016.09M-SP1-5 respectively.

parallel addition. This optimized MAC unit implementation can be extended for FIR filter applications.

TABLE I. DELAY AND POWER ANALYSIS FOR 8,16,32 BIT MAC

Width	8-bits	16-bits	32-bits
Delay (ns)	14.9	17.3	21.5
Power (mw)	0.225	0.648	4.795

TABLE II. RESOURCES USAGE OF 8,16,32 BIT MAC

Width	8-bits	16-bits	32-bits
LUT (out of 299544)	339	1625	4831
DFP (out of 299544)	51	98	65
User I/O (out of 244)	36	68	132

## VI. CONCLUSION

A unique optimized MAC unit with runtime reconfigurable multiplier is proposed targeting the reduction in computational complexity in multiplication along with an efficient hybrid adder network. Multiplier is designed reconfigurable using controller logic block that ensures the optimal resource reuse with reduction in power consumption and make it suitable for portable devices applications. An efficient adder that combines the CLA and conditional sum adder network that speeds up the addition operation by

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