"Design and Analysis of a 1.28 mW K-Band Modified Gilbert-Cell Mixer Using 22 NM FDSOI CMOS"

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***Abstract*—This paper presents a low-power, low-voltage down-conversion mixer fabricated in a 22 nm FDSOI CMOS technology. The proposed mixer design is based on Gilbert-cell architecture and uses a passive transformer instead of an active transconductance stage to overcome voltage headroom limitations in deep-sub-micron CMOS technologies. Measurement results show that the mixer achieves a voltage conversion gain of 7.8 dB, an input-referred 1 dB compression point of -7 dBm, and IIP3 of 4.8 dBm under -8 dBm local oscillator power. The mixer design consumes a low 1.28 mW of power from a single 0.8 V supply voltage, which is a significant improvement compared to the state-of-the-art. Furthermore, the mixer's compact size of 0.54×0.45 mm², including pads, makes it a highly attractive solution for various applications, as e.g. radar.**

***Index Terms*—FDSOI CMOS, down-conversion mixer, low power, low voltage, transformer, linearity.**

I. INTRODUCTION

Down conversion mixers play a crucial role in the RF front- ends of wireless systems, including 5G transceivers, short- range automotive radar devices, and many other applications. The modern down-scaled CMOS technologies enable front- end realization at mm-wave frequencies. This is due to improved f_t and f_{max}, which enable the integration of complex systems on the same chip area at a low cost.

On one hand, passive mixers offer such advantages as high linearity and zero DC power consumption, yet on the other hand, they suffer from conversion loss, which degrades overall system performance. Additionally, they require high local oscillator (LO) power, leading to increased DC power dissipation. However, in active mixers like a frequently used Gilbert-cell design [1], high conversion gain (CG), low noise, and good port-to-port isolation performances can be achieved at lower LO power, yet at the cost of lower linearity and DC power consumption. But, with deep sub-micron CMOS technology (e.g., 22 nm FDSOI process with 0.8 V), the Gilbert cell faces limitations due to stacked structures, which cause linearity degradation because of the limited rail-to-rail voltage headroom. To address this issue, several approaches have been proposed, such as employing folded mixer designs with current reuse shunt feedback as an RF stage [2] or using mixer designs with adaptive body effect control [3] to enhance the gain and noise performance.

In our previous work, we introduced a modified Gilbert-cell design that employs transmission lines as an RF stage and LO wave shaping to achieve high linearity and 1/f noise reduction [4], [5]. In this work, we build upon this idea and expand it by realizing the passive gm stage using a transformer as a RF stage to achieve a more compact design at the K frequency band with competitive performance in 22 nm FDSOI CMOS technology.

II. PROPOSED MIXER DESIGN

The schematic diagram of low-voltage down-conversion mixer design is illustrated in Fig. 1. The design uses two transformers to convert single-ended signals to differential and provide an ESD protection during measurement chip handling. Capacitors C_{T1} and C_{T2} are utilized to achieve matching at RF and LO inputs, while C_B acts as a DC block. LO inputs are biased using M_B diode-connected transistor and R_G resistors.

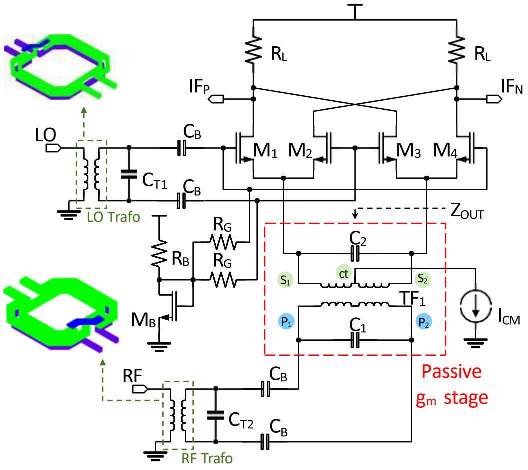

Fig. 1. Proposed low-voltage modified Gilbert-cell mixer design.

The mixer design is realized as a Gilbert cell with a modified RF stage. The transconductance stage of the mixer was removed and replaced with a transformer to mitigate the previously stated limitation in deep sub-micron CMOS technologies. The passive transconductance stage performs the RF voltage to current conversion. In addition, we used a low- voltage cascode current mirror I_{CM} (not shown in the design schematic) as a tail current source to improve the common mode, power supply rejection ratio, and avoid self-biasing effects.

The EM 3D layout of the passive transconductance stage transformer is illustrated in Fig. 2. The transformer windings are realized in the top thick metals available in the technology to minimize insertion loss. In order to have an accurate design, the transformer was simulated in RFpro ADS Momentum. The optimized EM simulation results show that the primary and secondary inductance at 30 GHz are 200 nH and 300 nH, respectively. Capacitors C_1 and C_2 are designed to achieve resonance at the operating frequency.

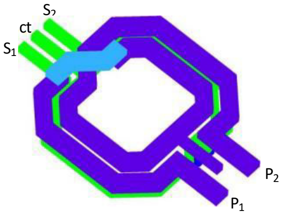

Fig. 2. 3D EM model of the transformer.

Small-signal simulation of the output impedance Z_{OUT} and the transconductance g_m of the passive transconductance stage are shown in Fig. 3. The presented curves shows that the output impedance is relatively high at the operating frequency, and the peak of the passive transconductance stage g_m at this frequency is around 16 mS.

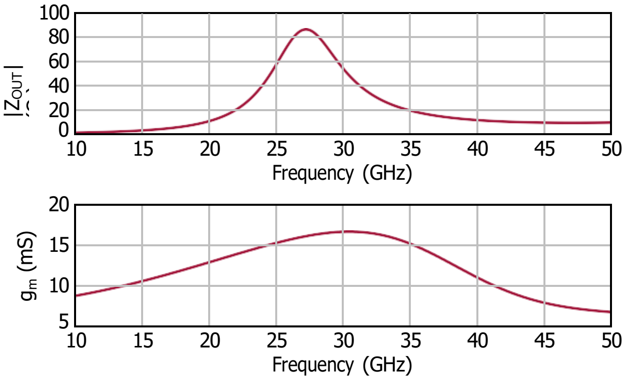

Fig. 3. Simulated output impedance and transconductance of the passive gm-stage over frequency.

The RF current is steered by LO switching quad M_{1-4} and converted to the voltage by the R_L load resistor. The switching quad transistor sizes are optimized to operate near the threshold voltage, which reduces the required driving LO power and noise contribution. For optimal performance, 16 fingers with a 2 µm width and minimum channel length were chosen for M_{1-4}, along with a load resistance of 400 Ω.

III. MEASUREMENT RESULTS

The proposed low-voltage mixer design was fabricated in the 22nm FDSOI CMOS technology from Global Foundries. The chip microphotograph and its 3D layout are depicted in Fig. 4. The area of the mixer, including pads, occupies 540×450 µm. The mixer core consumes 1.28 mW power from a single 0.8 V supply voltage.

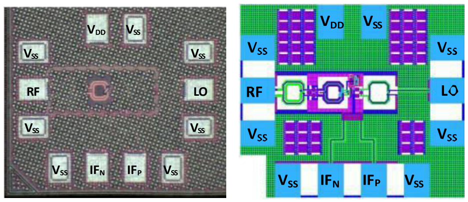

Fig. 4. The mixer chip photo and its 3D layout with pads (540µm × 450µm).

On-wafer S-parameter measurements were performed using MPI TS-200 THz probe station, a low noise Keysight E36312A DC supply, and a PNA Network Analyzer. As a calibration method, the short-open-load-thru (SOLT) technique was used. Fig. 5 shows the measured and simulated RF and LO input matching (S11) and isolation between these ports. The results indicate that the S11 values are lower than -10 dB, and isolation between RF and LO ports is around 50 dB at the operating frequency.

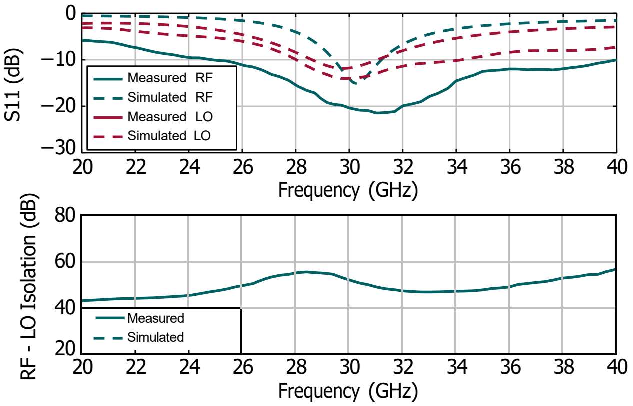

Fig. 5. Measured and simulated RF, LO return losses and isolation.

The mixer parameters were measured using an external buffer that can drive 50 Ω. Input RF and LO signals were fed by Keysight E8257D generators, and the output spectrum was observed by an R&S FSW85 spectrum analyzer.

The measured and simulated results of CG over LO power and IF frequency are shown in Fig. 6. After the de-embedding of cable losses, the measurement results show that the maximum CG can be achieved at -8 dBm LO power. However, the measured CG is slightly lower than the simulations due to losses on adapters and RF probes. Furthermore, the capacitive output of the external buffer leads to a decrease in IF bandwidth, which cannot be de-embedded.

The linearity measurements of the proposed mixer design are presented in Fig. 7. The measurements were performed with an LO power of -8 dBm. The input RF power of the mixer design at 1 dB compression point is -7 dBm, and the corresponding output power and CG are 0.6 dBm and 8.6 dB,

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE OF THE ART

Ref.	Technology	Supply (V)	RF (GHz)	CG (dB)	IP1dB (dBm)	IIP3 (dBm)	PLO (dBm)	SSB NF (dB)	PDC (mW)	Area (mm²)	Topology
This	22nm CMOS	0.8	24-34	7.8	-7	4.8	-8	16† / 12.3‡	1.28	0.243	Gilbert-cell + Passive g_m
[2]	130nm CMOS	1.5	23 - 25	26.1	-17.8	n.a.	-3	7.7	16.8	0.96	Folded Gilbert-cell + IF Buffer
[3]	65nm CMOS	1	26	7.2	-6.1	-2.5	5	12.3	10.3	0.4	Gilbert-cell DB + IF Buffer
[6]	22nm CMOS	1.2	25 - 31	12	-14.8	n.a	0	7-12	25	0.64	Single-balanced + IF Buffer

†Measured NF at 26GHz RF/LO frequency, ‡ Simulated NF at 30 GHz RF/LO frequency.

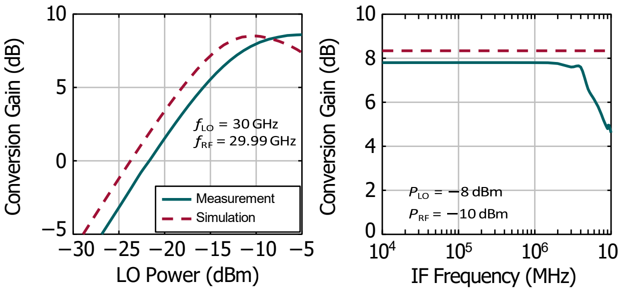

Fig. 6. Measured and simulated voltage CG versus LO power, and IF frequency.

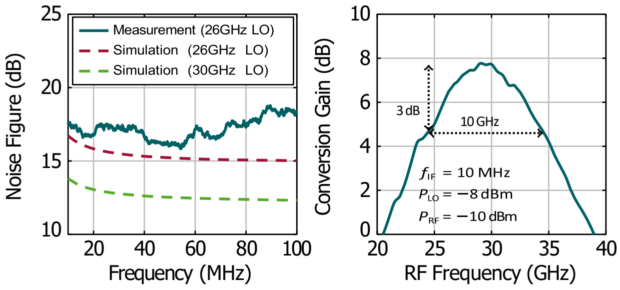

Fig. 8. Noise figure and conversion gain of the mixer.

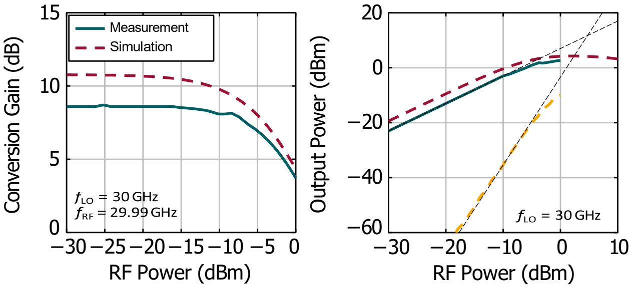

Fig. 7. Measured and simulated IP1dB and IIP3.

respectively. The measured input IP3 is about 4.8 dBm. The linearity of the measurement is higher than the simulated one, due to the lower CG of the fabricated mixer.

The single-sideband (SSB) noise figure has been measured at 26 GHz RF frequency and 26.01 GHz LO frequency by using Agilent 364C (10 MHz - 26.5 GHz) noise source and the spectrum analyzer. The 26 GHz RF frequency was chosen due to equipment limitations. Fig. 8 shows the measured and simulated results of the noise figure, which is 16 dB at an IF of 50 MHz. The mixer demonstrates the 3-dB bandwidth range from 24 to 34 GHz measured at constant IF at 10 MHz.

The measured parameters of the proposed mixer design are summarized and compared with other state-of-the-art mixer designs in Table I. The presented mixer design achieves low power consumption and high linearity at low LO power.

IV. CONCLUSION

The paper presents a modified Gilbert-cell down conversion mixer design, which operates at a low voltage and is fabricated in the 22 nm FDSOI CMOS technology. Using a passive transformer as an RF stage, the mixer is not only compact in size but also it has a very low power consumption of 1.28 mW, making it a highly suitable option for low-power applications compared to other state-of-the-art mixers.

ACKNOWLEDGMENT

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