Performance Analysis of Full Adder using Different CMOS Technology

N Sindhusree [1], N.Swathi [2], T.G. Tejaswini [3]

[1]PG Scholar, [2]Assistant Professor,[3]Assistant Professor, Dept of ECE, Anantha Lakshmi institute of technology & sciences, Anantapuramu.

***Abstract*—Very large-scale integrated (VLSI) circuits in the arithmetic logic unit depend heavily on extremely quick processing. Another crucial concern is lowering the power usage of physical tools. This paper presents a comprehensive performance analysis of full adders implemented using various CMOS technologies. The main target is evaluating key metrics such as power consumption and propagation delay. Different CMOS technologies, including 45 nm and 90 nm, are considered for the design and implementation of full-adder circuits. The number of transistors, delay time, and average power consumption in CMOS technology are significant determinants of integrated circuit performance and efficiency. The performance characteristics of these circuits are assessed through extensive simulation and analysis using Quartus II software and Cadence Virtuoso Tools. CMOS-based technology is used in this paper to achieve high speed and low power consumption.**

Keywords—full adder, average power, propagation delay, CMOS technology

I. INTRODUCTION

Today's integrated circuit designs are becoming more and more intricate. As technology advances, testing for increased performance can be done using circuit design methodologies. Very large-scale integrated (VLSI) circuits are electrical components designed with millions of transistors, like memory chips and microprocessors. A microelectronic circuit is created by putting millions of CMOS transistors onto a single chip using a technique called VLSI. The basic and most commonly used arithmetic function is the most speed-limiting component of many VLSI systems; therefore, maximizing its performance and power consumption is essential. The construction of a full adder utilizing CMOS (Complementary Metal-Oxide-Semiconductor) technology is a fundamental aspect of digital circuit design [1]. The chips' transistors and other component sizes are referred to as "nm technology." A chip can be faster and more energy-efficient if it is smaller in size, which is expressed in nanometers, or nm, and can accommodate more transistors. The main benefit of smaller technology nodes, such as those that are 32 nm, 45 nm, 90 nm, and so forth, is that they enable smaller transistors, which increase the number of transistors per unit area on a device. Higher performance may be possible as a result of increased integration. Although smaller technology nodes such as 32nm provide benefits like improved integration, reduced power consumption, and faster performance, they may have some difficulties, such as higher leakage currents and increased manufacturing complexity [2]. Full adders are integral components of digital systems' arithmetic and logical operations. They add three input bits and provide a sum and a carry output. A popular and efficient platform for building digital logic circuits is CMOS technology, which has low power consumption, strong noise immunity, and scalability [3]. A full adder designed with CMOS technology uses complementary pairs of p-type and n-type metal-oxide-semiconductor field-effect transistors (MOSFETs). It is required for addition to implement the logical functions. In the CMOS-based full adder design, consideration must be given to transistor sizing, layout optimization, power consumption, signal propagation delay, and overall circuit performance. Utilizing computer-aided design tools, simulation software, and a deep comprehension of the properties and behavior of CMOS devices are standard components of the design process. The focus is to provide robust, low-power, and high-performance operation within the parameters of contemporary integrated circuit design [4]. Related works are also described below. Shiva Sharma and Rajesh Mehra created two designs for full adders and two designs for 4-bit ripple carry adders based on 90 nm technology and compared them on the basis of area utilization and power consumption. From the simulations, the reduction of area by 17.02% and power by 2.07 % in Design2 as compared to Design1 and reduction of area by 35.03 % and power by 26.07 % in Design 'B' as compared to Design 'A' [5]. Sheenu Rana and Rajesh Mehra designed low power full adder with pass transistor logic which reduces the area, power and delay. The result showed that 8T full adder consumes 98% less power as conventional 28T and 65% less power compared to 16T full adder [6].

In this paper, a CMOS-based full-adder that uses the Cadence Virtuoso schematic tool and the Analog Design Environment (ADE L) tool to simulate timing waveforms is created. The complete adder circuit was first constructed using a NAND and XOR CMOS logic gate. Adder circuits were built and analyzed using CMOS technology at 45 nm and 90 nm. Following that, the timing waveform, power consumption, and propagation delay time of the entire design are examined. For better comprehension, the performance analysis table and graph are finally shown. The speed at which a full adder performs addition operations is essential for overall system performance. Therefore, minimizing propagation delay is a crucial focus in 45nm and 90nm full-adder designs.

There are five sections in this paper. A general introduction to full-adder IC design is given in Section I. The modeling of the complete adder architecture and theory is covered in Section II. The CMOS schematic is implemented in Section III. The simulation results and analysis of the system are described in Section IV, while the conclusion is provided in Section V.

II. Modeling of Full Adder Design

A. Full Adder

A basic full-adder has two outputs: Sum and Cout (carry out), and three inputs A, B, and Cin (carry in). Binary numbers include sum and Cout, as indicated in Table 1. The boolean equations associated with the fundamental logic diagram for a complete full adder are shown below.

$$\text{Sum} = A \oplus B \oplus C_{in} \quad (1)$$

$$C_{out} = AB + (A \oplus B).\, C_{in} \quad (2)$$

TABLE I. Truth Table for Full Adder

Input			Output	
A	*B*	*Cin*	*Sum*	*Cout*
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

B. Full Adder Design using NAND Gate

In digital circuit design, the full adder is a basic building component. It adds three input bits and produces a sum output and a carry output. The 1-bit full adder logic diagram is depicted in Figure 1 using Quartus II software [7].

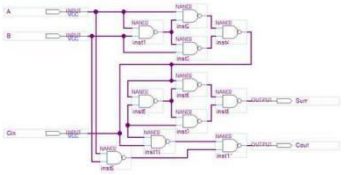

Fig. 1. Logic diagram of full adder using NAND gate.

C. Full Adder Design using XOR and NAND Gate

XOR and NAND gates are fundamental building blocks that are integrated to make a circuit that can add two binary values with a carry-in input in order to design a full adder. The logic diagram of full adder using XOR and NAND gate is depicted in Figure 2 using Quartus II software [7-9].

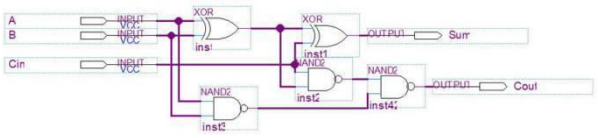

Fig. 2. Logic diagram of full adder using XOR and NAND gate.

D. Power Dissipation

Power dissipation is a measurement of the power consumed by the logic gate when all of its input is applied. The total power dissipation can be calculated using the equation below [10-11]:

$$P_{dynamic} = P_{switching} + P_{short\ circuit} \quad (3)$$

$$P_{switching} = CV_{DD}^2 f_{sw} \quad (4)$$

$$P_{static} = (I_{sub} + I_{gate} + I_{junct} + I_{contention})V_{DD} \quad (5)$$

$$P_{total} = P_{dynamic} + P_{static} \quad (6)$$

where:

C = dynamic effective capacitance

V_{DD} = voltage source

f_{sw} = switching frequency

E. Propagation Delay

A theoretical framework that takes into account several elements impacting signal propagation through the gate can be used to characterize the average propagation delay (t_p) of a logic gate in CMOS technology. Both the output load capacitance and the input transition time affect the average propagation delay. The following equation can be used to express the average propagation delay [12-13].

$$t_p = 0.69 \text{ x } R_p \text{ x } C_{load} \quad (7)$$

where:

t_p = Average propagation delay

R_p = Equivalent resistance seen by the output node of the gate

C_{load} = Total load capacitance at the output node of the gate

III. Creation of Full Adder Design

A. CMOS Technology

CMOS circuitry is superior to other types of circuitry in a number of ways, including reduced noise and process fluctuation sensitivity, faster operation, and lower power consumption. A p-channel MOS (pMOS) transistor and an n-channel MOS (nMOS) transistor are coupled in series-form CMOS technology, which is primarily advantageous because of its low power consumption. The four terminals of a CMOS transistor or device are the gate, source, drain, and body. Transistors of the p type and n type, pMOS and nMOS, function as switches. The output of a static CMOS gate is connected to logic "0" via a nMOS pull-down network (PDN) and logic "1" via a pMOS pull-up network (PUN), as shown in Figure 3. One of the networks is configured to be ON and the other to be OFF for a specific input pattern [12-13].

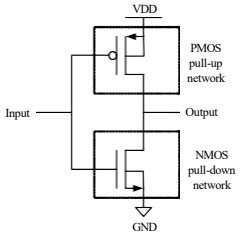

Fig. 3. Logic gate using pull-up and pull-down networks.

B. Full Adder Design with NAND Gate using 45 nm CMOS Technology

Figure 4 represents the 1-bit full-adder schematic in the Cadence Virtuoso tool, which is modelled using the 45 nm GPDK tool kit with a 1.8 V voltage supply and a 0.9 V threshold voltage. CMOS NAND gates are used to create a full adder.

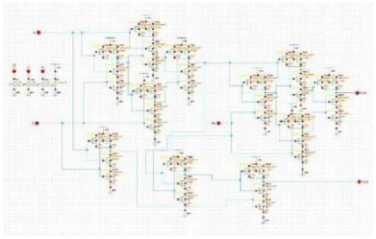

Fig. 4. Full adder schematic using NAND gate.

C. Full Adder Design with XOR and NAND Gate using 45 nm CMOS Technology

Figure 5 depicts the schematic for a full adder using XOR and NAND CMOS logic gate. In this design full adder created

using the CMOS process (18 pMOS and 18 nMOS), 36 transistors are used. PUN and PDN are linked by a fundamental structure. This schematic was produced using 45 nm technology by the Cadence Virtuoso tool.

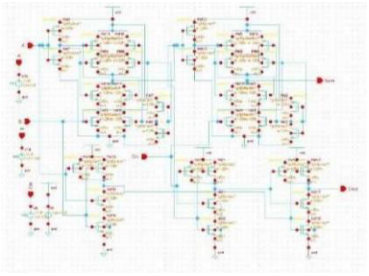

Fig. 5. Full adder schematic using XOR and NAND gate.

D. CMOS Full Adder Design with NAND Gate using 90 nm Technology

Figure 6 depicts the schematic for a full adder using NAND CMOS logic gate. In this design full adder created using the CMOS process (22 pMOS and 22 nMOS), 44 transistors are used. PUN and PDN are linked by a fundamental structure. This schematic was produced using 90 nm technology by the Cadence Virtuoso tool.

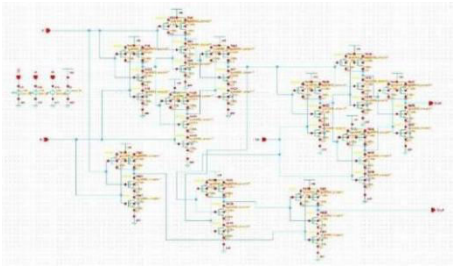

Fig. 6. Full adder schematic using NAND gate.

E. CMOS Full Adder Design with XOR and NAND Gate using 90 nm Technology

Figure 7 represents the 1-bit full-adder schematic in the Cadence Virtuoso tool, which is modelled using the 90 nm GPDK tool kit with a 1.8 V voltage supply and a 0.9 V threshold voltage. CMOS XOR and NAND gates are used to create a full adder.

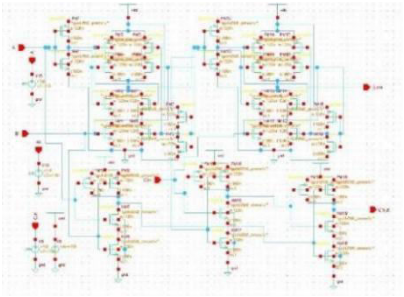

Fig. 7. Full adder schematic using XOR and NAND gate.

IV. Simulation Results

In this section, performance analyses of full adder designs are discussed. To validate the logic operations, schematic designs are simulated.

The output timing waveforms of the full adder designs are shown in Figures 8, 9, 10 and 11 below, respectively. The waveform is also simulated with 45 nm and 90 nm technology at 1.8 V supply voltage, and 300 ns stop times, respectively.

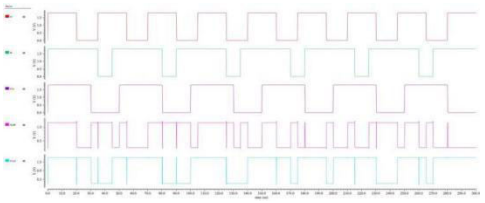

Fig. 8. Timing waveform of full adder design with NAND gate using 45 nm technology.

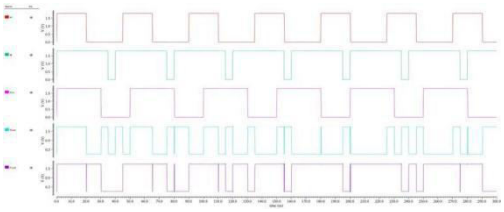

Fig. 9. Timing waveform of full adder design with XOR and NAND gate using 45 nm technology.

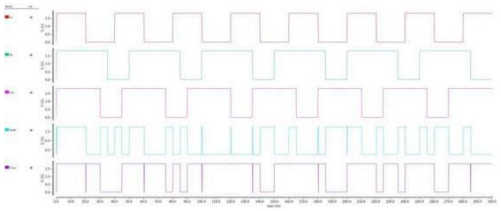

Fig. 10. Timing waveform of full adder design with NAND gate using 90 nm technology.

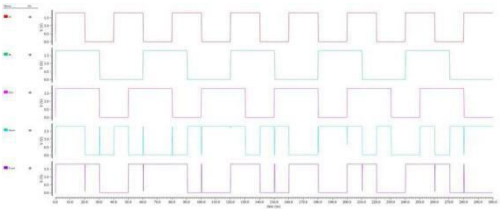

Fig. 11. Timing waveform of full adder design with XOR and NAND gate using 90 nm technology.

In the graphs of average power calculation in Figures 12, 13, 14 and 15, the power consumed by the 45 nm and 90 nm CMOS-designed circuit is shown. The average power consumption of Figures 12 and 13 using 45nm technology is 1.0858 µW and 0.908278 µW, respectively. It has been discovered that the XOR full-adder architecture has lower power usage. Figures 14 and 15 have average power consumptions of 5.73189 µW and 4.93977 µW, respectively, using 90nm technology. It has been demonstrated that the XOR full-adder architecture uses less electricity. All levels have a constant threshold voltage of 0.9 volts. This voltage marks the moment when power and current start to increase as the supply voltage rises. Operating temperatures have been specified for all designs at 27°C.

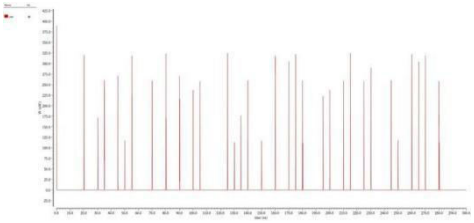

Fig. 12. Power consumption of full adder design with NAND gate using 45 nm technology.

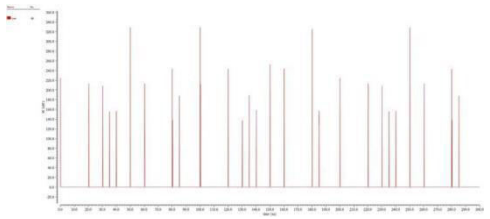

Fig. 13. Power consumption of full adder design with XOR and NAND gate using 45 nm technology.

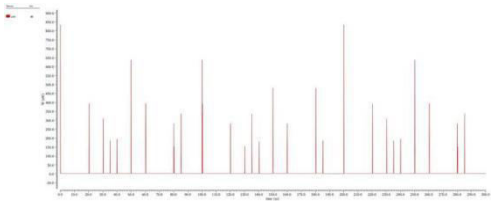

Fig. 14. Power consumption of full adder design with NAND gate using 90 nm technology.

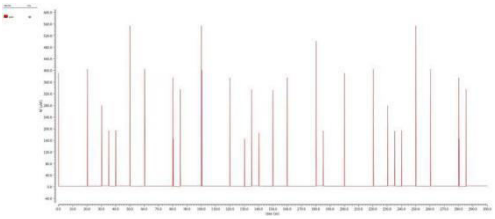

Fig. 15. Power consumption of full adder design with XOR and NAND gate using 90 nm technology.

Figures 16, 17, 18 and 19 analyzes the average power and propagation delays of the full adder design. According to the ADE L simulation results, the delay of 12.0002 psec and 22.4814 psec of full adder designs using 45nm technology are shown in Figures 16 and 17. It was found that the delay time of the NAND-only full adder design is less. Figures 18 and 19 show the delay of 19.0855 psec and 24.0832 psec for full-adder designs using 90nm technology. It is found that the delay of the NAND-only full adder design is less. The design simulation was carried out using Cadence Virtuoso in the ADE L environment.

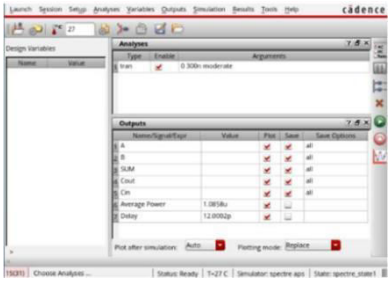

Fig. 16. Average power and delay of full adder design with NAND gate using 45 nm technology.

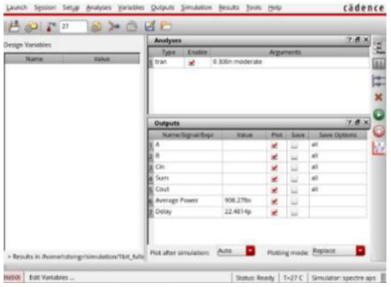

Fig. 17. Average power and delay of full adder design with XOR and NAND gate using 45 nm technology.

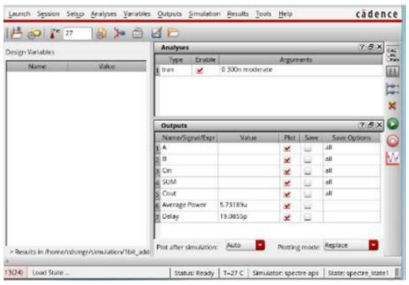

Fig. 18. Average power and delay of full adder design with NAND gate using 90 nm technology.

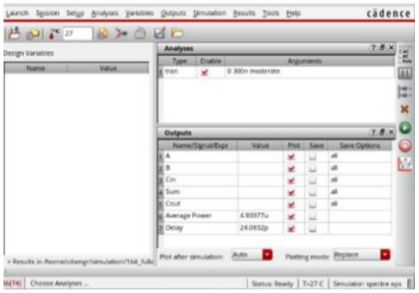

Fig. 19. Average power and delay of full adder design with XOR and NAND gate using 90 nm technology.

Table 2 and 3 displays a comparison between full adder NAND and full adder XOR performance. It involves the total number of transistors, average power and propagation delay. The NAND-only full adder design uses eleven NAND gates (the conventional NAND gate uses 4 transistors), thus using a total of 44 transistors. A total of 36 transistors are used in the XOR full-adder architecture, which consists of two XOR gates (a conventional XOR gate needs 12 transistors) and three NAND gates (a conventional NAND gate uses 4 transistors). The Cadence Virtuoso was used for the simulations and design.

TABLE II. FULL ADDER USING NAND GATE

Parameters	CMOS Technology	
	45 nm	***90 nm***
Average Power (in µW)	1.0858	5.73189
Delay (in p sec)	12.0002	19.0855
Transistor Count	44	44

TABLE III. FULL ADDER USING XOR AND NAND GATE

Parameters	CMOS Technology	
	45 nm	***90 nm***
Average Power (in µW)	0.908278	4.93977
Delay (in p sec)	22.4814	24.0832
Transistor Count	36	36

The full adder design comparative analyses are depicted graphically in Figures 20 and 21. Figure 20 shows the bar graph of the performance analysis of a full adder using NAND gates of various 45nm and 90nm technologies. In terms of average power and delay, 45nm technology design performs better than 90nm technology design since the

average power and delay are lower. Figure 21 shows the bar graph of the performance analysis of a full adder using XOR gates of various 45nm and 90nm technologies. Since 45nm technology has lower average power and delay than 90nm technology, it performs better in terms of average power and delay.

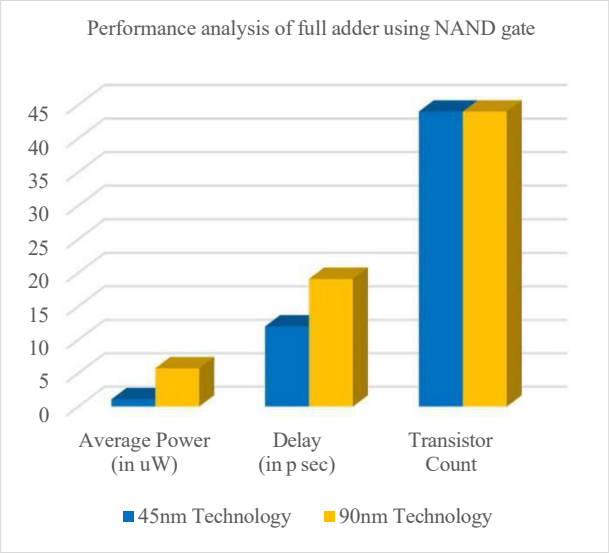

Fig. 20. Parametric summary of full adder using NAND gate.

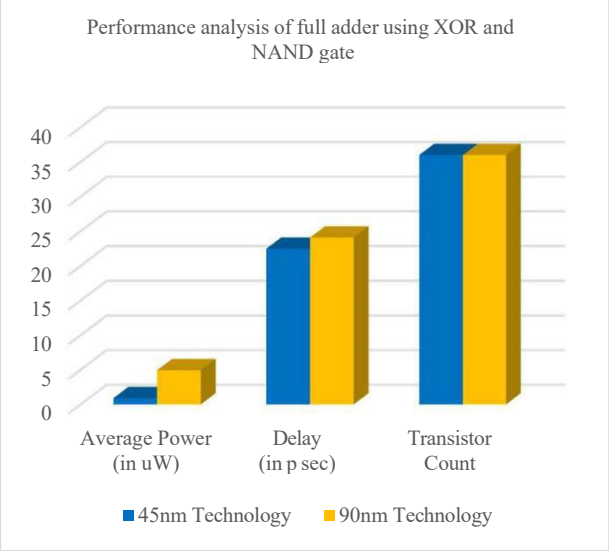

Fig. 21. Parametric summary of full adder using XOR and NAND gate.

V. Conclusions

A schematic analysis and comparison of average power and propagation delay have been conducted for the design of a full adder based on 45 nm and 90 nm technology. For 45 nm technology, two designs of full adders have average power consumptions of 1.0858 µW and 0.908278 µW, respectively. The propagation delay times are 12.0002 ps and 22.4814 ps, respectively. For 90 nm technology, two designs of full adders have average power consumptions of 5.73189 µW and 4.93977 µW, respectively. The propagation delay times are 19.0855 ps and 24.0832 ps, respectively. Analyzing the adder circuits using the Cadence Virtuoso tool, it was found that the propagation delay of the NAND gate full adder is 46.6217% less at 45nm and 20.7518% less at 90nm compared to the XOR gate full adder. The number of transistors increases, but with low power consumption and high speed. These findings demonstrate the advantages of designing and implementing sophisticated digital circuits using 45 nm CMOS technology, which provides improved performance metrics critical to today's electronic systems.

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