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CNTFET-Based Digital Arithmetic Circuit Designs in Ternary Logic with Improved Performance and Energy Efficiency

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Abstract*— Ternary logic, a type of multi-valued logic (MVL), offers notable advantages over traditional binary logic in terms of circuit density, power efficiency, and computational performance. This paper proposes a novel design for a ternary full adder (TFA), which is developed using an optimized ternary half adder (proposed THA). The TFA circuits are implemented using carbon nanotube field-effect transistors (CNTFETs), which are highly suitable for MVL systems due to their ability to support multiple threshold voltages. The proposed THA design plays a key role in improving the overall performance of the TFA by significantly reducing transistor count, power consumption, and propagation delay. The entire system is modeled and simulated using HSPICE with Stanford's 32nm CNTFET technology at a supply voltage of 0.9V. Simulation results confirm the efficiency of the proposed circuits, showcasing improvements in energy consumption, speed, and accuracy. These advancements make the design a promising solution for future nanoscale arithmetic operations and energy-efficient computing platforms.

Keywords—Ternary Half Adder, Ternary Full Adder, HSPICE

I. INTRODUCTION

The electronics industry is currently placing a great deal of emphasis on the integrated circuit miniaturization process. This results in a decrease in the circuits' physical footprint and increased operational efficiency [1-3]. Regarding this issue, the semiconductor industry continuously aims to reduce the size of metal-oxide-semiconductor transistor (MOSFET) dimensions by half because, according to Moore's law, this will essentially double the number of transistors contained on the chip [4]. A number of significant obstacles and complications face the MOSFET device as it moves toward the sub-32 nm technological node[5]. These include a variety of short channel effects (SCEs), low gate control over the channel, high power density, notable parametric fluctuations, and increased subthreshold leakage current [6]. The cumulative consequence of these problems is to deteriorate transistor performance and reduce its suitability for use in energy-efficient applications [6]. To overcome these problems, it is therefore essential to develop alternate transistor technology solutions. Similar to MOSFETs, carbon nanotube field-effect transistors (CNTFETs) exhibit improved performance and energy efficiency, which has generated significant interest. The distinct electrical features of CNTFET devices offer a viable foundation for designing circuits and systems at the nanoscale [7,8]. Devices that use inputs and outputs with two distinct states are known as binary logic gates. '0' or '1', which represent 0V or VDD, respectively. In electronic devices like computers and calculators, these gates are widely used and represent the foundation of the digital world [9]. Their use does, however, have a significant drawback in that more connections lead to more complicated circuits that take up a lot of chip space and use more energy and power [10-11]. Digital electronic devices known as multiple-valued logic (MVL) gates, on the other hand, are made especially for system states greater than two. In addition to providing significant benefits in data compression, MVL gates also minimize the number of interconnects needed for intricate operations [12]. The best basis has been found to be e=2.718, but due to hardware constraints, an integer base that roughly approximates e must be used, and three seems to be the number that does show [13,14]. By employing three-valued logic, ternary logic can reduce chip size and energy by up to 70% and 50% , respectively[15].

The below figure illustrates the structure of a multi-channel Carbon Nanotube Field Effect Transistor (multi-CNTFET). In the front view (Fig. 1(a)), the device is built on a substrate, over which a bulk dielectric layer is deposited to provide insulation. A gate dielectric layer is placed above this, separating the gate electrode from the channel region. The central gate controls the flow of current between the source and drain terminals, which are located on either side of the gate. Doped Carbon Nanotubes (CNTs) serve as the channel material and connect the source and drain, allowing for electron transport when a voltage is applied at the gate.

The top view (Fig. 1(b)) shows the layout of the transistor, highlighting several key parameters. The gate is centrally placed between the source and drain, with the channel length (Lch) denoting the distance over which the CNTs span between these terminals. Lightly Doped Drain (Ldd) and Lightly Doped Source (Lss) regions are included to improve device performance and reduce short-channel effects. The gate width (Wgate) and the pitch between adjacent CNTs are also shown, which are critical in determining the current-driving capability and integration density of the device. This multi-CNTFET structure offers promising features for nanoscale

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electronics, including high-speed operation and low power consumption.

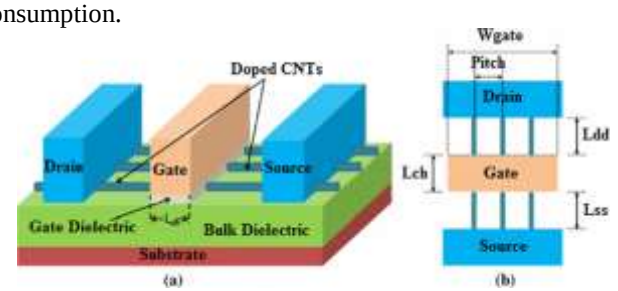

Fig. 1 A multi-CNTFET, (a) Front-view and (b) Top-view

As stated in [18], the multi-threshold voltages (Vth) approach is the proper technique for designing and implementing ternary circuits. Body biasing is a well-known technique for achieving multi-threshold designs in a MOSFET.CNTFETs, circuits with multiple Vth may be developed and implemented: the required Vth is obtained by taking appropriate CNT diameters into account [4]. This research proposes an enhanced design for THA and TMUL based on CNTFETs. The suggested THA/TMUL designs reduced the number of transistors by 54.44%/45% respectively as an effective factor on the delay and power, improving the latency, power, and PDP by 37.01%/30.48%,14.07%/6.64%, and 45.87%/36.74%, respectively, in comparison to their earlier iterations, i.e., [10,20].

II. LITERATURE REVIEW

Multi-valued logic (MVL), and in particular ternary logic, represents a significant advancement beyond traditional binary systems by employing three distinct logic levels instead of two. The foundational concept of ternary logic dates back to the early theoretical models proposed by Thomas Fowler in the 19th century, with increasing practical interest emerging as a response to the growing limitations of binary circuit complexity, chip area, and power consumption in large-scale integration systems . Ternary logic, often classified into balanced {-1, 0, +1} or unbalanced {0, 1, 2} forms, has attracted considerable attention because it offers improved information density and energy efficiency . The unbalanced ternary approach, which maps three logic states to voltage levels {0 V, VDD/2, VDD}, is especially favored in circuit realizations for its practical hardware implementation advantages .In the domain of ternary arithmetic circuits, half-adders, full adders, multipliers, and related modules have seen diverse implementation methodologies. Early approaches primarily leveraged conventional CMOS technology, which encountered challenges related to increased interconnect complexity, power dissipation, and scaling issues inherent to binary logic extensions . To tackle these concerns, researchers explored novel circuit structures, such as ternary multiplexers without decoders, ternary unary-functions, and logic synthesis algorithms aimed at reducing transistor counts and enhancing switching speed Later designs incorporated emerging technologies including resistive random-access memory (RRAM) in conjunction to ternary logic to improve power-delay products (PDP) and area efficiency . Advances in multiplier circuits similarly emphasized compact design and energy efficiency by exploiting ternary logic's higher radix to achieve data compression and reduce the number of required operations .

III. METHODOLOGY

1. CNTFET

CNT are small, cylindrical graphic structures that fall into one of two types: single-walled (SWCNT), which has a single cylinder, or multi-walled (MWCNT), which has two or more cylinders [21,22]. The chirality vector, which is an integer pair denoted by (n,m), determines how the carbon atoms are oriented throughout the length of a SWCNT. SWCNTs have the ability to act as conductors or semiconductors [23]. If the numerical difference between n and m equals 3k, where k is an integer with a value of +ve. The SWCNT is suitable for the interconnect network and performs the role of a conductor. On the other hand, the SWCNT behaves like a semiconductor and can be used in a FET channel if n minus m is not equal to 3k [21]. In Fig.1, the multi-CNTFET is illustrated. The CNTFET, like the CMOSFET, has a Vth that actuates the gate to activate the device. What makes CNTFETs different, though, is that they can only determine the Vth by using appropriate CNT diameter sizes. More alternatives for digital circuit designs are provided by this special feature, which even allows for the fabrication of multi-Vth circuits. A CNTFETs Vth can be expressed using eq. (1) [24,25].

$$v_{th} \cong \frac{Eg}{2e} = \frac{\sqrt{3}}{3}\frac{av_{\Pi}}{eDC_NT} \cong \frac{0.43}{D_{cNT}} \qquad (1)$$

where Vπ≅3.033eV is the π-π band energy of carbon in tight bonding model, a=0.249nm is gap between carbon atoms, e is electron-charge, and DCNT is CNT diameter, that is calculated by Eq. (2)

$$D_{cNT} = \frac{a\times\sqrt{n^2xm^2+nm}}{\pi} \cong 0.783\sqrt{n^2+m^2+nm} \qquad (2)$$

CNTFET Device	Chiral Value(n,m)	Vth	VGS(V)		
			0	0.45	0.9
P-type	(10,0)	-0.56v	ON	OFF	OFF
	(19,0)	-0.29v	ON	ON	OFF
N-type	(10,0)	0.56v	OFF	OFF	ON
	(19,0)	0.29v	OFF	ON	ON

Table. 1 The Vth values and ON/OFF conditions of CNTFETs, categorized based on the chiral values employed

The gate width (WGate) of a CNTFET is defined by Equation (3), where it depends on the pitch the spacing between carbon nanotubes—and the number of nanotubes (ntube) used in the device

$$WGate = pitch \times (n_{tube} - 1) + D_{cNT} \qquad (3)$$

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Carbon nanotube field-effect transistors (CNTFETs) have evolved into several distinct device structures, each tailored to a specific performance–power trade-off. In Schottky-barrier (SB) CNTFETs, a direct metal–CNT contact at the source–channel interface forms a Schottky barrier that enables carrier tunneling but inherently restricts transconductance and on-state current. In contrast, band-to-band tunneling (BTBT) CNTFETs exploit tunneling across the nanotube bandgap, delivering excellent cut-off behavior and ultra-low power operation at the cost of reduced on-state current, which makes them highly suitable for subthreshold and energy-constrained applications. To overcome these limitations, MOSFET-like CNTFETs introduce heavily doped CNT regions at the source and drain to eliminate the Schottky barrier, significantly enhancing on-state current and switching speed, and thereby emerging as a strong candidate for future high-performance, ultra-high-speed digital circuits.Table 1 lists the requirements for the ON and OFF states of CNTFETs [5]. According to the data, a CNT with chiral values of (10, 0) has a high threshold voltage of 0.56 V, whereas a CNT with chiral values of (19, 0) has a low threshold voltage of 0.29 V

Operations	**Expressions**
OR	$x_i + x_j = max(x_i, x_j)$
AND	$x_i . x_j = min\{x_i, x_j\}$
NOT	$\bar{x_i} = 2 - x_i$

Table. 2 Basic ternary operations

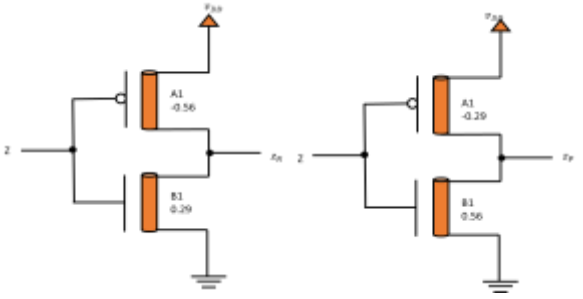

Fig. 2 Circuit diagrams of the (a) NTI and (b) PTI [5].

1.1. Ternary System

Ternary logic, proposed by Thomas Fowler in 1840, uses three values instead of binary. It can be balanced ({-1, 0, 1}) or unbalanced ({0, 1, 2}), with this study focusing on the unbalanced mode represented by voltage levels {0V, VDD/2, VDD}. Basic ternary systems rely on universal gates and inverters, governed by equations in Table 2. Three inverter types—standard (STI), positive (PTI), and negative (NTI)—are used, with PTI and NTI schematics shown in Figure 2 and their equations detailed in Equation 4.

$$x_N = \begin{cases} 0, if\ x \neq 0 \\ 2, if\ x = 0 \end{cases} \quad (4a)$$

$$x_P = \begin{cases} 2, if\ x \neq 2 \\ 0, if\ x = 2 \end{cases} \quad (4b)$$

$$\bar{x} = 2 - x \quad (4c)$$

Equations (5a) and (5b) formally specify the two-input ternary NAND (TNAND) and ternary NOR (TNOR) functions for inputs A and B in the cited work.

$$\text{TNAND} = \overline{min\{A, B\}} \quad (5a)$$

$$\text{TNOR} = \overline{max\{A, B\}} \quad (5b)$$

Several CNTFET-based ternary half adder (THA) and ternary multiplier (TMUL) designs have been reported, using a wide range of design strategies. These include pure conventional logic implementations, conventional logic enhanced with RRAM, and architectures built by cascading ternary multiplexers (TMUXs) or ternary gates (TGs). Other approaches rely on ternary unary-functions combined with TMUXs or TGs, logic synthesis algorithms, or mixed and alternative design styles that selectively integrate these techniques to optimize performance and resource usage.

1.2. CNTFET-Based ternary Circuits:

Ternary circuits with CNTFETs Effective ternary arithmetic scheme design using CNTFETs, such as THA and TMUL, is covered in this section.

1.3. Half – Adder:-

The Ternary Half Adder (THA) is a digital circuit with two inputs (A and B) and two outputs (sum and carry). It performs addition in ternary logic. Jaber et al. implemented the THA by starting from a conventional expression (Equation 6), commonly used in prior works [15,36], and derived a new form (Equation 7) to optimize the design. The corresponding truth table is provided in Table 3.

Input		Output	
A	B	sum	carry
0	0	0	0
0	1	1	0
0	2	2	0
1	0	1	0
1	1	2	0
1	2	0	1
2	0	2	0
2	1	0	1
2	2	1	1

Table. 3 THA truth table

1.4. Multiplexer Based Ternary Half Adder

A 3:1 multiplexer is a combinational circuit that routes one of three inputs *((I_0), (I_1), (I_2))* to a single output (B), based on the values of its selection lines. It enables controlled data selection from multiple sources.

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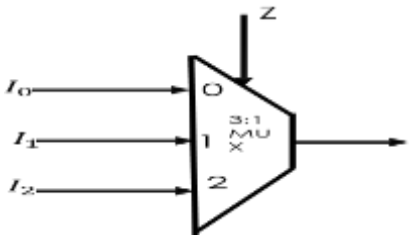

Fig. 3 Circuit of ternary multiplexer, (a) Symbol .

A Ternary Multiplexer (TMUX) is a digital circuit that selects one of three inputs *(I_0, I_1, I_2)* using a ternary control signal Z with logic levels 0, 1, or 2. It is especially useful in multivalued logic systems, enabling efficient data selection beyond binary constraints.

The operation of a TMUX is defined as follows:

- When Z = 0, the output (B) equals I0.
- When Z = 1, the output (B) equals I1.
- When Z = 2, the output (B) equals I2

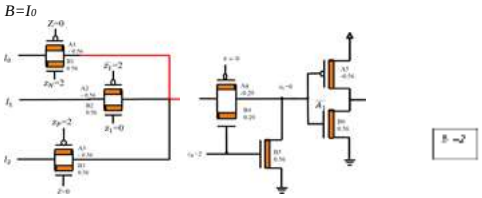

Fig..4 Circuit of ternary multiplexer, (a) Symbol and (b) Transistor-level structure [10].

Table .4 Selection Table

Z	B
0	*I0*
1	*I1*
2	I_2

1.5. Ternary Half Adder :

The ternary half adder (THA) circuit is an improved design built entirely from transistors. It overcomes previous limitations by using only PCNTFET and NCNTFET devices, which share the same threshold voltage due to identical chirality vectors and mobility. The NCNTFET passes strong logic 0, while the PCNTFET passes strong logic 1 and 2. By identifying each transistor's chirality vector, the design optimizes performance, achieving a 54.44% reduction in transistor count (using just 41 transistors) and improvements of 8.78% in delay, 44.07% in power, and 53.42% in energy efficiency.

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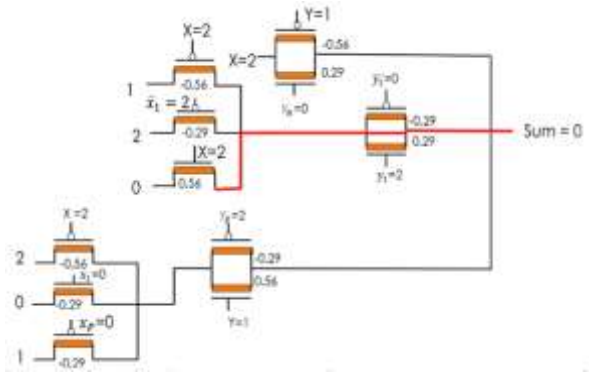

Fig. 5(a): Circuit of THA(Sum)

The above fig(a). shows the proposed THA Sum circuit. To illustrate the operation of the proposed ternary half adder, consider the input combination X = 2 and Y = 1. In this case, the transistors highlighted in red demonstrate the conduction path that leads to the output Sum = 0. At a threshold voltage of 0.29 V, both PCNTFET and NCNTFET are turned ON for logic values 0 and 2, enabling the corresponding paths in the circuit. Additionally, the NCNTFET associated with the logic value 2 becomes active at a threshold voltage of 0.56 V, ensuring the connection to the output node. As a result of these conduction

paths, the circuit outputs a sum value of 0, as expected for this input combination.

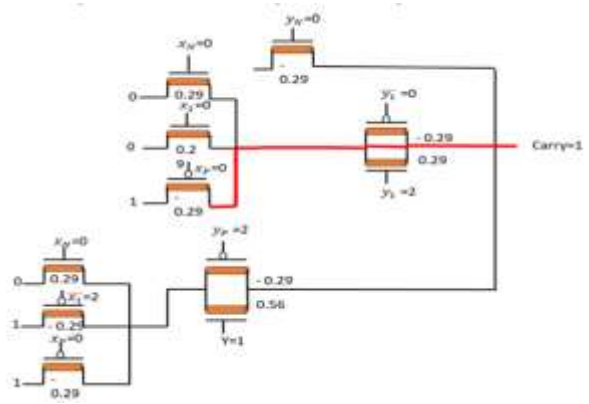

Fig. 5(b) Circuit of THA(Carry)

The above fig(b). shows the proposed THA Carry circuit. To illustrate the generation of the carry output, consider the input combination X = 1 and Y = 2. The conduction path responsible for producing Carry = 1 is highlighted in red in the circuit diagram. At a threshold voltage of 0.29 V, both PCNTFET and NCNTFET transistors corresponding to logic levels 0 and 2 are turned ON, allowing current to flow through the designated path. Additionally, the PCNTFET associated with the logic level 0 also becomes active at -0.29 V, completing the conduction path toward the carry output. As a result, the circuit correctly produces the output Carry = 1 for this input condition. This approach can similarly be used to verify the sum & carry outputs for all other input combinations.

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2. Carry Generator :

A carry generator is a crucial component in digital arithmetic circuits, especially in multi-bit adders, where it ensures accurate addition by managing carry propagation between digit positions. It activates when the sum of two digits exceeds the base, generating a carry to the next higher bit. In the given example, with inputs A = 0 and B = 1 (mapped to AN = 2 and BN = 0), the circuit uses PCNTFET and NCNTFET transistors operating at specific threshold voltages to determine the carry output. The correct ON/OFF states of these transistors—based on logic levels and threshold voltages—lead to a final carry output of 1. This confirms the circuit's proper functionality for the tested input, demonstrating the effectiveness of the carry generator in handling ternary logic operations.

A	B	Output
0	0	0
0	1	1
0	2	1
1	0	1
1	1	2
1	2	2
2	0	1
2	1	2
2	2	2

Table. 5 Truth table for Carry Generation

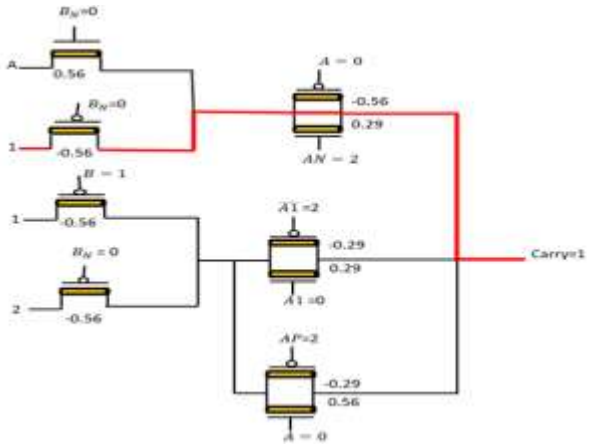

Fig.6 Circuit diagram of carry Generator

2.1 Ternary Full Adder:

Ternary full adder is an arithmetic circuit that operates with three logic values: 0, 1 & 2. It extends the concept of binary addition by handling three valued inputs making it more efficient than binary adders. It takes three inputs A, B & C and produces two outputs as sum and carry.

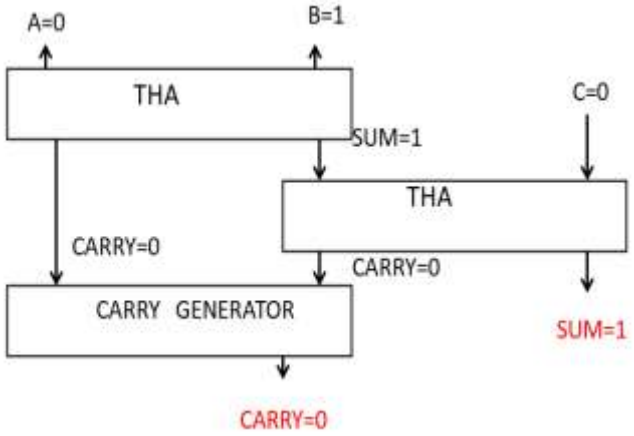

Fig. 7 Block diagram of ternary full adder.

Illustrates the block diagram represents a ternary full adder (TFA), which performs addition in ternary logic (values: 0, 1, 2) instead of traditional binary logic (values: 0, 1). The circuit consists of two Ternary Half Adders (THA) and a Carry Generator. The first THA takes two ternary inputs, A and B, and produces a SUM and an intermediate CARRY. This SUM output is then fed into the second THA along with the third input, C, to compute the final SUM and another intermediate CARRY. The Carry Generator processes the carry signals from both THAs to produce the final CARRY output. This ternary full adder plays a crucial role in ternary arithmetic circuits, which offer advantages in terms of reduced power consumption and higher computational efficiency compared to binary systems. For the input combination A = 0, B = 1, and C = 0 in a Ternary Full Adder (TFA), the circuit operates as follows. The first Ternary Half Adder (THA) receives inputs A = 0 and B = 1, producing a SUM of 1 and a CARRY of 0. This SUM output (1) is then fed into the second THA along with the third input C = 0, resulting again in a SUM of 1 and a CARRY of 0. The final step involves the Carry Generator, which takes the two carry outputs from the THAs (both 0 in this case) as inputs. Referring to the Carry Generator truth table, the input combination (0, 0) yields an output of 0. Thus, for the given inputs, the final output of the TFA is a SUM of 1 and a CARRY of 0, consistent with the expected behavior based on the TFA block diagram and the Carry Generator logic. The TFA is designed by using multiplexers, i.e., a MUX-based full adder. Compared to the MUX-based design, the proposed transistor-only Ternary Full Adder (TFA) achieves significant improvements: a 51.58% reduction in transistor count, a 44.07% decrease in power consumption, an 11.50% reduction in delay, and a 56.20% enhancement in energy efficiency (EDP). this work introduces a **CNTFET-based Ternary Full Adder (TFA)** that integrates two Ternary Half Adders (THA) with a Carry Generator to process three-valued inputs {0,1,2}. The proposed architecture leverages the strengths of CNTFET devices and ternary logic to deliver improvements in power consumption, delay, and overall energy efficiency. With its compact and low-power design, the proposed TFA represents a step toward highly efficient

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arithmetic circuits for next-generation nanoscale and energy-constrained computing platforms

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	0	2	2	0
0	1	0	1	0
0	1	1	2	0
0	1	2	0	1
0	2	0	2	0
0	2	1	0	1
0	2	2	1	1
1	0	0	1	0
1	0	1	2	0
1	0	2	0	1
1	1	0	2	0
1	1	1	0	1
1	1	2	1	1
1	2	0	0	1
1	2	1	1	1
1	2	2	2	1
2	0	0	2	0
2	0	1	0	1
2	0	2	1	1
2	1	0	0	1
2	1	1	1	1
2	1	2	2	1
2	2	0	1	1
2	2	1	2	1
2	2	2	0	2

Table. 6 Full Adder Truth Table

2.2 Simulation Setup:

The proposed CNTFET-based Ternary Full Adder (TFA) was designed and verified using **HSPICE** simulations with the **Stanford 32 nm CNTFET model**. The supply voltage (**VDD**) was fixed at **0.9 V**, ensuring compatibility with nanoscale device operation. The CNTFET parameters, including chirality vector, tube diameter, and channel length, were carefully selected to achieve multiple threshold voltages (Vth) required for implementing ternary logic {0,1,2}. Both p-type and n-type CNTFETs were utilized to construct the two Ternary Half Adders (THAs) and the Carry Generator, which together form the complete TFA architecture. Simulation experiments focused on validating both **functional accuracy** and **performance efficiency**. Functional verification was carried out through transient analysis to confirm correct **Sum** and **Carry** outputs for all possible ternary input combinations. Performance evaluation involved extracting critical design parameters such as:

- **Average Power Consumption (nW):** measured during continuous operation of ternary inputs.
- **Propagation Delay (ps):** time required for the output response after input transition.
- **Power–Delay Product (PDP, zJ):** representing energy efficiency of computation.
- **Energy–Delay Product (EDP, qJs):** combining power, energy, and delay factors.

Transistor Count: total devices used in implementation, indicating circuit complexity.

IV. SIMULATION AND VERIFICATION RESULTS

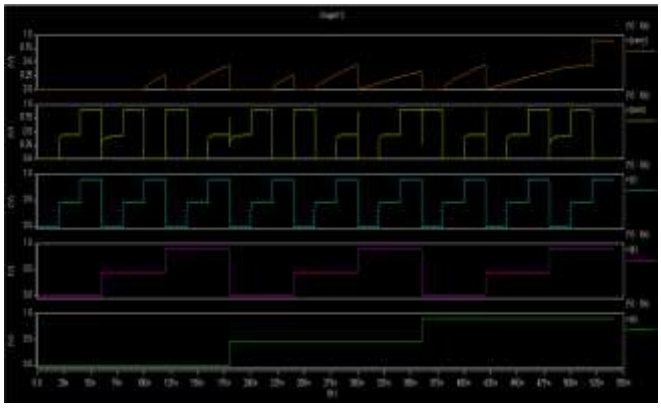

Fig.8 Simulation outputs for Ternary Full Adder

Ternary Half-Adder	Power (n W)	Delay (p s)	PDP (z J)	EDP (q Js)	No.of Transistors
Mux-based	37.952	79.957	3034.5	242.63	90
Transistor-level	21.23	72.952	1548.7	112.98	41

Table.7 Comparision for Ternary Half Adder

Ternary Full-Adder	Power (n W)	Delay (p s)	PDP (z J)	EDP (q Js)	No.of Transistors
Mux-based	37.952	79.952	3034.5	242.63	190
Proposed	21.226	70.752	1501.7	106.98	92

Table. 8 Comparision for Ternary Full Adder

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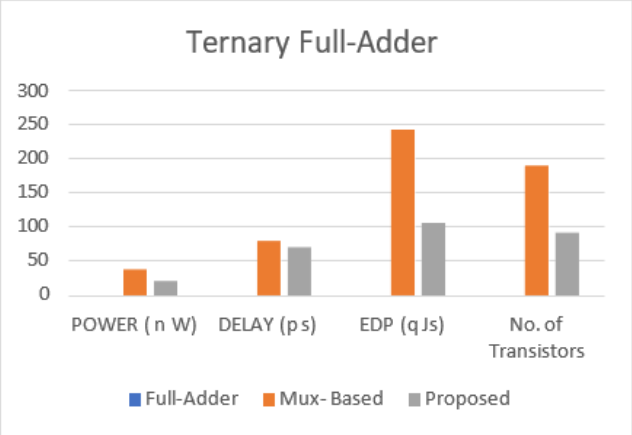

Fig.9 Results for Ternary Half-Adder

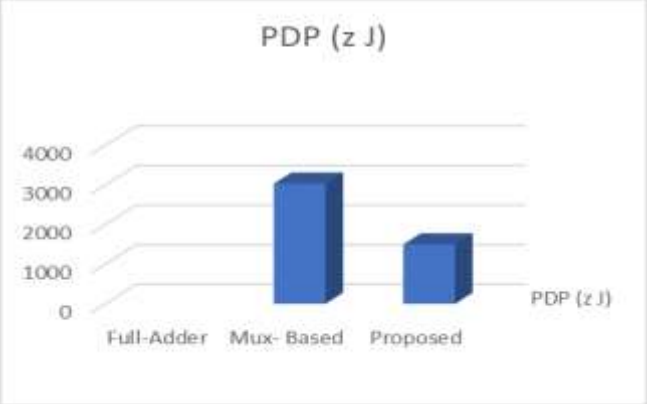

Fig.10 PDP for Ternary Full-Adder

V. CONCLUSION

This research successfully developed and tested new ternary logic-based arithmetic circuits such as half adders, full adders, and multipliers using Carbon Nano Tube Field Effect Transistors (CNTFETs).By exploring multi-valued logic, especially ternary logic, the study aimed to address limitations of traditional binary systems like high power usage, larger chip size, and complex wiring. Thanks to CNTFETs' unique voltage properties, the proposed designs were optimized and evaluated through simulations, showing impressive improvements. Compared to conventional designs, these circuits used fewer transistors and achieved significant reductions in power consumption, delay, and energy metrics. Overall, the results highlight the potential of CNTFET-based ternary logic to enable more efficient and compact computing systems, paving the way for future advancements in nanoscale technology.

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