A LOW-LATENCY PIPELINE CORDIC-BASED CARRIER DISCRIMINATOR DESIGN AND IMPLEMENTATION FOR GPS AND NAVIC SIGNAL TRACKING

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ABSTRACT
To estimate carrier phase and keep in sync with received satellite signals, Global Navigation Satellite System (GNSS) receivers—such as GPS and NavIC—need precise carrier tracking. Using the in-phase (I) and quadra (Q) correlator outputs, the carrier discriminator calculates phase error, which it then provides to the carriers tracking loop. Phase estimation frequently uses the four-quadrant arctangent operation atan2(Q,I), however its hardware implementation may result in a multi-cycle processing delay or a lengthy combinational path. A low-latency, pipelined CORDIC-based carrier discrimination algorithm for tracking GPS and NavIC signals is presented in this study. A coordinate-rotating computer (CORDIC) core divided into pipeline stages is used in the suggested design. The shift-add computations are distributed using intermediate registers and iteration scheduling. The correlator, the integrate-and-dump unit, code detector, and code generator are kept, but the discriminator output is linked to the current carrier loop filter and quantitatively controlled oscillator (NCO). The architecture is designed for functional verification with Xilinx Vivado 2026 and Verilog HDL implementation.1. Logic utilisation, power, maximum operational frequency, processing lag, and phase-estimation error are examples of evaluation measures. Before being published, any numerical examples that are given must be substituted with measurable implementation reports.

KEYWORDS
GNSS, GPS, NavIC, pipelined structure, phase estimation, a PLL, Verilog HDL, carrier tracking, carrier identifier, CORDIC.

I. INTRODUCTION

Precision agriculture, transportation, surveying, telecommunications, and defence are just a few of the uses for which Global Navigation Satellite Systems offer positioning, navigation, and timing services. Satellite signals are transmitted via GPS and India's NavIC system, and a receiver processes them to estimate position, velocity, and time. Prior to calculating navigation parameters, a GNSS receiver usually performs radio-frequency processing, acquisition, tracking, and analog-to-digital conversion [1], [2].

The receiver continuously aligns spreading-code and locally generated carrier copies with the incoming satellite signal during tracking. Correlators, integrate-and-dump accumulators, carrier and code discriminators, loop filters, and numerically driven oscillators are common components of the tracking architecture. The carrier tracking loop can function as a frequency-locked loop (FLL), phase-locked loop (PLL), or both [1], [3]. I and Q, the quick correlator's in-phase and quadrature components, are produced. These elements are transformed into an error measurement using a carrier phase discriminator. Atan2(Q,I) is a popular four-quadrant phase discriminator; however, depending on the receiver architecture and signal modulation, Costas-loop implementations may employ atan(Q/I) [4]. To update the carrier NCO, the discriminator output is filtered. CORDIC is an iterative arithmetic method that uses additions, subtractions, and shifts to compute functions like sine, cosine, and arctangent. It can eliminate the requirement for general-purpose multipliers, which makes it appealing for digital hardware [5], [6]. When the CORDIC method is in vectoring mode, it spins an input vector in the direction of the horizontal axis while calculating the angle. The cumulative angle can serve as the phase estimate for I/Q inputs.

A sequential CORDIC solution minimises hardware replication by reusing a single processing stage for several repetitions, but it takes multiple cycles to generate an output. Several input vectors can be processed simultaneously thanks to an unrolled or pipelined architecture, which divides iterations among hardware stages. To prevent a single, lengthy critical path and needless register overhead, the stage allocation must be balanced [6], [7].

In order to minimise the processing delay related to the I/Q-to-phase conversion, this work offers a pipelined CORDIC carrier discriminator. The optimised iteration scheduler assigns CORDIC iterations to pipeline stages in groups. Together with the intermediate X, Y, and Z values, the scheduler maintains iteration order and transmits the necessary valid and control information.

The GNSS carrier tracking loop incorporates the suggested discriminator. The correlator creates early, prompt, and late branches; integrate-and-dump generates I/Q values; the code discriminator and code loop filter update the code NCO; and the carrier loop filter updates the carrier NCO. The surrounding receiver functions do not change. The suggested modification to the carrier discriminator is isolated by this modular method.

II. RELATED WORK

Basics of GNSS Receiver and Tracking [1], [2]. GNSS signal structure, receiver processing, acquisition, and tracking loops are explained by Kaplan and Hegarty. The receiver context that carrier discriminators, loop filters, and NCOs function in is established by their treatment. The

functions of integrate-and-dump, discriminators, filters, and local oscillators are similarly explained in the Navipedia tracking-loop overview. Discriminators for Carrier Tracking [3], [4]. PLL and FLL discriminator selections and their reaction to phase and frequency faults are described in carrier tracking literature. The arctangent discriminator is employed in Costas-loop designs, whereas the atan2(Q,I) discriminator offers four-quadrant phase information. Modulation, noise, and tracking circumstances must be taken into account while choosing the discriminator. Tracking of Weak-Signal Carriers [5]. Weak-signal carrier tracking research examines noise behaviour and discriminator gain as carrier-to-noise density drops. These findings demonstrate that signal strength, integration time, loop architecture, and arithmetic accuracy all influence phase-estimation performance.

Algorithm CORDIC [6]. Volder developed the CORDIC method, which uses iterative shift-and-add operations to compute trigonometrics. The approach gives a hardware vectoring engine that calculates an I/Q vector's angle its mathematical foundation.

CORDIC in general [7]. Walther expanded the CORDIC approach to include a larger class of simple functions. The generalised formulation guides the choice of iteration constants and coordinate updates and offers a basis for rotation and vectoring modes.

Hardware Architectures for CORDIC [8]. Hu reviewed digital signal processing VLSI architectures based on CORDIC. The architecture decisions and trade-offs that affect hardware cost, throughput, and implementation complexity are covered in the paper.

Implementations of FPGA CORDIC [9]. Andraka examined the architecture and implementation aspects of CORDIC algorithms for FPGA-based computers. The work facilitates the use of CORDIC for devices that can be configured for digital signal processing.

CORDIC with High Speed and Low Power [10]. Five decades of CORDIC algorithms, designs, and applications were examined by Meher and colleagues. Techniques for increasing performance and power efficiency are covered in their assessment, including pipeline organization and architecture-level optimisation.

Baseband GNSS Processing [11]. The GNSS-ISE study finds carrier discriminator computations like atan2(Q,I) and explains receiver baseband processes. It shows that the discriminator is an appropriate target for hardware acceleration since it is a unique computational activity in a GNSS processing chain.

GNSS Carrier Discriminator FPGA [12]. A carrier discriminator that is implemented as part of a GNSS tracking channel and requires atan(y,x) is described in published FPGA receiver work. The work provides a pertinent verification method by reporting phase-error deviation and comparing hardware discriminator results against a floating-point reference.

Tracking Architectures for NavIC [13], [14]. NavIC L5 and S-band readings are used in recent NavIC studies to examine vectorised and carrier-aided tracking. These investigations emphasise the necessity of robust tracking mechanisms and accurate carrier-phase measurements in NavIC receivers.

Proposed Scheduling and Pipelining [6], [8], [10]. According to research on CORDIC architecture, pipelining can boost throughput by enabling various vectors to occupy distinct phases. In order to balance stage delay while keeping the current GNSS tracking-loop blocks, the suggested work particularly applies this idea to the carrier discriminator and introduces iteration grouping.

III. PROPOSED SYSTEM

The suggested method uses a pipelined CORDIC-based phase estimator in place of the traditional carrier discriminator arithmetic block. The entire GNSS receiver is not redesigned. The receiver design still includes the RF front-end, ADC, correlator, integrate-and-dump unit, code discriminator, code loop filter, code generator, carrier loop filter, and carrier NCO.

A. I/Q and Input Interface Samples: Signed I and Q samples are provided by the integrate-and-dump unit and prompt correlator. The received prompt correlation vector is represented by these values. In order to monitor each accepted vector through the pipeline, the input interface simultaneously records I and Q and associates them with a valid signal.

B. Pre-processing and Scaling: The I/Q values are scaled to the internal fixed-point format and their sign is verified prior to CORDIC vectoring. While maintaining adequate fractional precision, scaling should prevent overflow. Since the phase of a zero-vector situation (I=0 and Q=0) is indeterminate, it must be handled explicitly.

C. Pipelined CORDIC Core: Vectoring iterations are carried out by the CORDIC core. The direction of rotation at iteration i is determined by the sign of the residual Y value. Arithmetic shifts and addition/subtraction are used to update the X and Y coordinates, and Z accumulates the corresponding arctangent constant. Subject to the selected angle format and quadrant convention, the estimated phase is represented by the final Z value.

D. Optimised Iteration Scheduling: Pipeline stages are mapped to groups of the total number of iterations. Instead of allocating iterations without considering their timing, the scheduler seeks to balance the combinational delay of each stage. To maintain the mathematical vectoring sequence, the iteration order and related constants must not change.

E. Pipeline Registers: To hold X, Y, Z, valid, and any necessary sign or quadrant metadata, registers are added in between iteration groups. There must be precisely the same number of pipeline stages between the valid signal and the data. Back-to-back input vectors and reset behaviour need to be confirmed.

F. Phase Error Output: The phase estimate is adjusted in accordance with the quadrant convention and pre-processing after the last CORDIC stage. The carrier loop filter receives the resulting phase error. The carrier NCO, which creates the local carrier replica that the correlator uses, receives a correction command from the loop filter.

G. GPS and NavIC Tracking Integration: Only the carrier discriminator path contains the suggested block. The code discriminator and early, prompt, and late correlation data are still used in the code tracking path. In addition to

keeping the suggested adjustment localised, this enables independent evaluation of the carrier discriminator prior to complete receiver integration.

H. Fixed-Point Design and Verification: Documentation is required for the input width, internal coordinate width, fractional bits, iteration count, and arctangent constants. For all quadrants, axis-aligned inputs, modest magnitudes, and representative noisy vectors, a self-checking testbench should compare the output phase with a high-precision atan2(Q,I) reference.

The provided block diagram highlights the suggested pipelined CORDIC carrier discriminator and shows the entire GNSS signal tracking loop. The pipelined vectoring datapath and optimised iteration scheduling within the discriminator are the suggested contributions; the remaining tracking-loop blocks are kept.

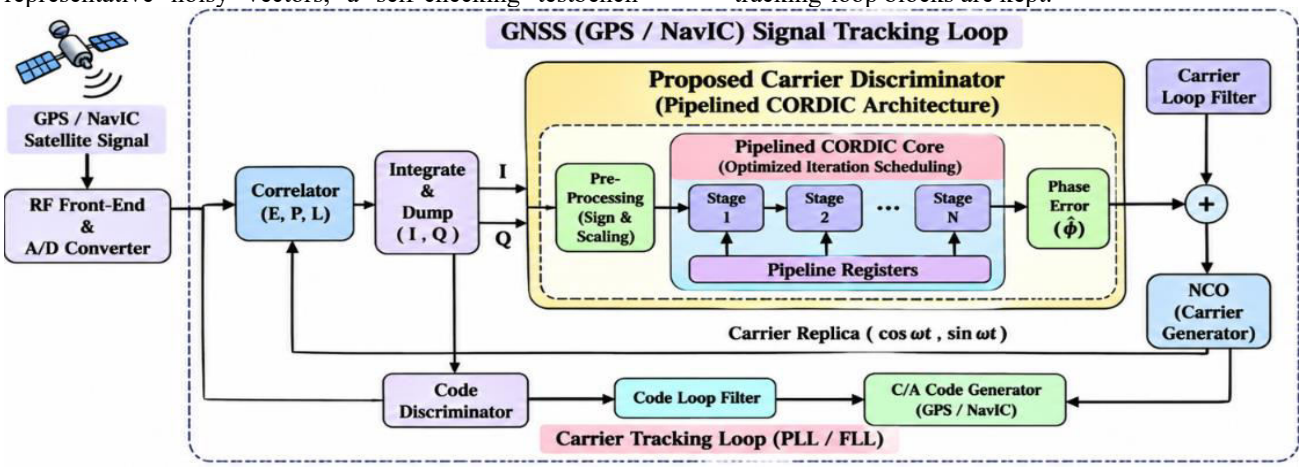

Fig. 1. GNSS GPS/NavIC signal tracking loop with proposed pipelined CORDIC-based carrier discriminator.

Verilog modules for I/Q pre-processing, CORDIC iteration stages, pipeline registers, phase correction, iteration scheduler, and a top-level carrier discriminator comprise the implementation. Clock, reset, input-valid, signed I/Q inputs, phase output, and output-valid should all be part of the top-level interface. This discriminator can be connected to the carrier loop filter and NCO via the entire receiver top module.

IV. RESULTS AND DISCUSSION

The following comparison shows how the traditional and suggested carrier discriminator architectures can be reported using illustrative example values. These figures are not measured Xilinx Vivado results; rather, they are estimations for paper presentation. Before publication, they must be replaced with real synthesis, implementation, timing, and power reports.

Because CORDIC iteration groups are spread over several stages, the suggested pipelined architecture is anticipated to require more flip-flops and logic. In exchange, pipelining is meant to speed up the acceptance of I/Q samples and reduce the combinational critical path. The chosen FPGA device, fixed-point word length, iteration count, and stage allocation all affect the precise trade-off. Both architectures employ the same CORDIC iteration count and signed I/Q input format for the illustrative comparison. Table I provides a summary of the estimated resource and timing values. The reciprocal of the assumed critical-path delay is used to determine the maximum frequency. The clock frequency and the presumptive commencement interval are used to assess throughput. The example shows that the suggested design has a greater target throughput, a shorter critical path, and a higher register utilisation. Because more pipeline registers and repeated stage logic may result in increased switching and clock load, the projected power value is likewise larger. Clock enables, switching activity, location, routing, and device features can all affect actual power.

When both architectures employ the same coordinate width, fractional precision, iteration count, angle constants, and rounding technique, phase-estimation accuracy should stay same. Fixed-point outputs must be compared to a high-precision atan2(Q,I) reference in order to determine the maximum phase error displayed in the table, which is merely an example goal.

TABLE I. ILLUSTRATIVE PERFORMANCE COMPARISON

Parameter	Conventional CORDIC	Proposed Pipelined CORDIC
I/Q input width	16-bit signed	16-bit signed
CORDIC iterations	16	16
Architecture	Iterative vectoring	Pipelined vectoring with optimized scheduling
LUTs (estimated)	480	690
Flip-flops (estimated)	120	280
DSP blocks (assumed)	0	0
Power (estimated)	0.072 W	0.089 W
Critical-path delay (estimated)	28.4 ns	16.8 ns

Maximum frequency (calculated)	35.21 MHz	59.52 MHz
Processing latency (assumed)	16 cycles	5 cycles
Initiation interval (assumed)	16 cycles	1 cycle
Throughput (calculated)	2.20 MSamples/s	59.52 MSamples/s
Maximum phase error (illustrative target)	≤ 0.15°	≤ 0.15°

V. CONCLUSION AND FUTURE SCOPE

A low-latency pipelined CORDIC-based carrier discriminator for tracking GPS and NavIC signals was introduced in this study. The suggested architecture uses an optimised iteration schedule to distribute the iterative shift-add operations around pipeline stages and applies CORDIC vectoring to the prompt I/Q correlator outputs.

The suggested change is restricted to the carrier discriminator. The code discriminator, code loop filter, code generator, correlator, integrate-and-dump unit, carrier loop filter, and NCO are kept. In order to handle several I/Q vectors in an overlapping way, pipeline registers carry the intermediate coordinate and control information.

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