AN ENHANCED SENSE-AMPLIFIER FLIP-FLOP USING CONDITIONAL BOOSTING TECHNIQUE

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ABSTRACT: Conventional high-performance flip-flops suffer from large power consumption at the nominal supply region and unreliable operation in the low-voltage region. To overcome these drawbacks, this paper proposes conditional-bridging flip-flops (CBFFs) that can conditionally activate the shorting device in the sense-amplifier stage. There are two versions of the proposed flip-flop. The single-ended version (CBFF-S) adopts a single-ended latching stage to optimize in terms of power consumption and area. For applications requiring high speed with differential outputs, the speed-optimized differential version (CBFF-D) is also proposed. Since the shorting device is adaptively turned on only when it is necessary, the flip-flops have fully static operations with reduced switching power consumption. The conditional bridging technique can also help minimize the effective parasitic capacitance relevant to the shorting device by relieving the design burden of weakening the device, resulting in further power reduction. The technique also provides the complete separation of complementary precharge nodes in the sense-amplifier stage during input sampling, achieving a fast and reliable operation. To further reduce power consumption and latency, the latching stage is designed to have no glitches and signal fighting and to be driven by the first stage output without signal inversion. Moreover, the conditionally bridged sense-amplifier stage having a reliable pull-down of precharge nodes and the latching stage having a contention-free operation allow the flip-flops to provide stable operation down to the near-threshold voltage (NTV) region. The proposed flip-flops were designed in a 28-nm CMOS process, whose performance evaluation results indicated that the power consumption of CBFF-S is reduced by up to 56.2% compared to conventional single-ended flip-flops at 0.1 switching activity. The minimum DQ latency was also reduced by up to 33.6%. They also indicated that CBFF-D offers up to 33.8% less power at 0.1 switching activity and up to 24.1% lower minimum DQ latency than those of conventional differential flip-flops. The resulting power-delay product (PDP) of CBFFs was at least 27.8% less than those of conventional flip-flops. The Monte-Carlo simulation results considering the process, voltage, and temperature (PVT) variations indicated that CBFFs could operate reliably down to a supply voltage of 0.3 V.

INDEX TERMS: Flip-flop, pulsed latch, sense amplifier, high performance, low power, low voltage.

I. INTRODUCTION

As stated by International Technology Roadmap for Semiconductor power consumption is considered as one of the important challenge in VLSI along with speed and area consideration. Different ways for reducing the power consumption have been proposed. In all these challenging methods minimizing power supply voltage gives direct and effect on reducing power consumption [1]. Flip flops are major building blocks in digital VLSI system. The applications areas where flip flops are majorly used are in registers, pipelines, state machines for sequencing data. Flip flop have direct impact on power consumption and speed of VLSI system. Flip flop and latches consume more power becauseof redundant transitions & clocking system which is included in it. Thus our aim is to design high performance and also power efficient flip flop. One of the challenging methods to design low power flip flop is to use sub threshold technology. Power consumption of circuit depends on several factors such as data activity, frequency, supply voltage, capacitance leakage and short circuit current. The total power dissipation is given by the sum of static and dynamic power dissipation. Amongst them dynamic power is one of the important and it is given by,

$$P_{Dynamic} = 0.5.\ CL.VDD^2.f \quad \text{..... (1)}$$

Where α is the probability of signal transition within clock period, CL is the load capacitance, VDD is the power supply voltage, f is clock frequency. Hence by reducing the power supply voltage there is tremendous reduction in power consumption of circuit. When supply voltage VDD reduces below the transistor threshold voltage VT, it is said to operate in sub threshold region. This is one of the efficient methods for low power application in which the performance is of secondary importance [2][3]. As power supply voltage is reduced below the transistors supply voltage VT, the sub threshold current slowly charges and discharges nodes for circuits logic function. This weak driving current limits the performance but low energy operation can be achieved with reduced dynamic &leakage power, resulting in improving battery life. In sub threshold region due to absence of conducting inversion channels, transistors behave differently than in strong inversion region. Thus resulting circuit characteristics change accordingly. Sub threshold technology can be used in various applications such as wearable medical equipments such as hearing aids & pace makers, wrist watch bursty mode application, which is ideal for a long period of time. In sub threshold circuit it satisfies the ultra power requirement. The reason behind this is that it uses leakage current for its operating switching current. This small leakagecurrent however affects the performance at which the circuit is operated. Portable electronic devices require energy-efficient computation to get a long operation time with lean power budget. Voltage scaling is one of the effective approaches to minimize the power consumption of CMOS digital circuits [1]. Unfortunately, aggressive voltage scaling such as subthreshold computing causes

severe speed degradation. To minimize energy while considering latency, the near-threshold computing appears as a viable solution [2]. However, still increased latency and performance variability of circuits operating in the nearthreshold voltage range may be unacceptable in many applications requiring high speed and low power. For example, for clocked timing elements such as latches and flip-flops [3]–[7] that constitute major circuit components in high-speed synchronous systems, performance parameters such as latency, setup time, and hold time will be degraded and have a large variation if they are operated in the nearthreshold region, resulting in undesirable effects on the overall system performance. Capacitive boosting [8]–[10] can be a solution to overcome the problems caused by aggressive voltage scaling. It allows the gatesource voltage of some MOS transistors to be boosted above the supply voltage or below the ground. The enhanced driving capability of transistors thus obtained can reduce the latency and its sensitivity to process variations. The bootstrapped CMOS driver presented in [8] relies on this technique to drive heavy capacitive loads with substantially reduced latency. However, since it is a static driver, every input transition causes the bootstrapping operation. So, if some of the transitions are redundant, a large amount of redundant power consumption may occur. The conditional-bootstrapping latchedCMOS driver [9] proposes the concept of conditional bootstrapping to eliminate the redundant power consumption. As it is a latched driver, it can allow boosting only when the input and output logic values are different, resulting in no redundant boosting and improved energy efficiency, especially at low switching activity. Recently, a differential CMOS logic family adapting the boosting technique has also been proposed for fast operation at the near-threshold voltage region [10]. Pipelining is an important design technique to realize highperformance digital systems. In a pipelined system, a large combinational logic block is broken down into a series of smaller blocks separated by pipeline registers. Composed of several flip-flops in parallel, these pipeline registers synchronize the flow of data from one stage to the next. Deeply pipelined systems break down the combinational logic block to a greater extent, so that each pipeline stage encapsulates a simple operation. As one example, we have integrated deep pipelining into the design of a medium-grain reconfigurable architecture for digital signal processing [1]. This architecture features an array of 4-bit cells and a hierarchical interconnection network. Each cell and interconnection level forms one pipeline stage. Clearly, deeply pipelined systems face several challenges: numerous pipeline registers, a large clock distribution network, and increased power consumption [2]. The delay overhead of the pipeline registers also becomes more significant as the number of stages increases and clock frequencies scale upward. The register delay may actually approach the pipeline stage delay, greatly reducing the available time for computation. For all these reasons, high-speed and low-power flip-flops are essential to sustaining high throughput in deeply pipelined systems. Most flip-flops only generate a single-ended output, using an inverter to supply the complement if

required. The extra inverter carries a speed penalty and places the two signals out of alignment. On the other hand, differential flip-flops generate both outputs simultaneously. This alternative is especially beneficial to combinational elements such as decoders and multiplexers, where misaligned signals might cause glitches later in the circuit. Circuit styles such as pass-transistor logic also achieve better performance with symmetric signals. Thus, differential flip-flops are a reasonable choice for deeply pipelinedsystems. With the scaling of transistors, maintenance of power consumption of VLSI chips has been increasing. Moore's Law drives VLSI technology to continuous enhances in transistor densities and higher clock frequencies. The developments in VLSI technology scaling in the preceding few years reveal that the number of on-chip transistors has been increased by 40% every year. The operating frequency of VLSI systems increases approximately 30% every year. Although capacitances and supply voltages are decreasing meanwhile, a power consumption of the VLSI chips is raising continuously. In contrast, cooling systems cannot improve as rapid as the consumption of power increases. Therefore, in the very close future chips are expected to have limitations of cooling system and solving this problem will be expensive and inefficient. Flip-flops (FFs) are the most commonly used memory elements for electronic circuits. Many electronic circuits employ several FF-rich modules like register files, shift registers, and first in first out systems (Hwang et al.; 2012). It is figured out that the clock distribution circuits and memory elements are consumed40-45% of the total consumption of power. FFs thus contribute a fairly huge segment of the chip area and consumption of power to the overall system. Pulse-triggered FF (PTFF), because of its single-latch structure, is generally used than the conventional master–slave based FFs and transmission gate FFs in high-speed applications. Apart from the speed advantage, its circuit simplicity reduces the consumption of power of the clock distribution system. A PTFF comprises of a clock pulse generator and a latch for data processing. If the triggering pulses in clock pulse generator are sufficiently narrow, then latch performs like an edge-triggered FF. Pulse generation methods can be categorized as implicit and explicit triggered method (Lin; 2014). In an implicit-type PTFF, the pulse is generated within the flip flop, and no explicit pulse signal yields, but in an explicit-type PTFF, pulse generator and latch are separately utilized. Low-voltage circuit design has been widely investigated for ultra-low power applications, reaching as low as 230mV in a recent multi-pipelined processor [39], and requiring wide-range level conversion for communication with I/O pads and high-voltage circuit blocks. Inaddition, cores on a chip multiprocessor are increasingly voltage scaled independently [9],necessitating *level conversion between core voltage domains in high performance applications. Another example is a multi-core system in [41], which suggests an optimal voltage/frequency mapping among the cores and requires thousands of level converters (LCs). LCs become more critical as the voltage difference grows, for instance, between aggressively voltage-scaled DSP

accelerators [13] and I/O. An extreme case is the wireless sensornode platform in [7], where the core is operated at a sub-threshold level while sensors and radio use the battery voltage (3.6V). Due to such significant voltage differences, these applications require wide-range LCs with fast and low power operation. However, level conversion is challenging at reduced voltages since conventional approaches suffer from severe contention between weakpull-down devices and strong pull-up devices, making them vulnerable to process / voltage / temperature (PVT) variations. Also, LCs in many sensing applications, such as environmental monitoring, will be exposed to extreme conditions, exacerbating robustness challenges in the LCs.

II. LITERATURE REVIEW:

"Self-Timed Pulsed Latch for Low-Voltage Operation With Reduced Hold Time

A self-timed pulsed latch (STPL) is proposed for low VDD operation. By comparing input and output, the transparency window is adaptively generated in STPL, which resolves the hold time problem of the conventional pulsed latch. The measurement results from the test chip fabricated in the 65-nm technology proves that the hold time is reduced by 77% and the minimum operating supply voltage is lowered by 300 mV compared with the conventional pulsed latch. In addition, the measurement results show that the STPL can reduce the sequential overhead, because the STPL is free from setup time issue from which the conventional master-slave-based flip-flop (MSFF) suffers. The simulation results show that the input-to-output delay of STPL, which also determines the sequential overhead, is smaller by 45% in 0.6 V compared with that of the MSFF structure.

A Variation-Tolerant Differential Contention-Free Pulsed Latch with Wide Voltage Scalability,"

As the dynamic power of electronic circuits has a quadratic dependence on the supply voltage (VDD), scaling VDD is the most effective approach to achieving low power consumption. Thus, flip-flops that can operate in a wide voltage range (from near threshold to super threshold) with minimum performance degradation are essential. However, in the near-threshold voltage (NTV) region, sequencing elements (flip-flops) suffer from unacceptably increased sensitivity to process variation, which results in significant speed degradation and functional failure. To solve the speed degradation problem, a pulsed latch can be used instead of conventional master-slave flip-flop. Thanks to its negative or near-zero setup time due to time borrowing, addition timing overhead due to setup time variation can be significantly reduced with a pulsed latch [1–2]. However, prior art pulsed latches suffer from functional failure in the NTV region because of challenging pulse-width control along with variations.

"Improved sense-amplifier based flip-flop: design and measurements,

Design and experimental evaluation of a new sense-amplifier-based flip-flop (SAFF) is presented. It was found that the main speed bottleneck of existing SAFF's is the cross-coupled set-reset (SR) latch in the output stage. The new flip-flop uses a new output stage latch topology that significantly reduces delay and improves driving

capability. The performance of this flip-flop is verified by measurements on a test chip implemented in 0.18 /spl mu/m effective channel length CMOS. Demonstrated speed places it among the fastest flip-flops used in the state-of-the-art processors. Measurement techniques employed in this work as well as the measurement set-up are discussed in this paper.

A novel high speed sense-amplifier-based flip-flop,"

A new sense-amplifier-based flip-flop is presented. The output latch of the proposed circuit can be considered as an hybrid solution between the standard NAND-based set/reset latch and the NC-/sup 2/MOS approach. The proposed flip-flop provides ratioless design, reduced short-circuit power dissipation, and glitch-free operation. The simulation results, obtained for a 0.25-/spl mu/m technology, show improvements in the clock-to-output delay and the power dissipation with respect to the recently proposed high-speed flip-flops. The new circuit has been successfully employed in a high-speed direct digital frequency synthesizer chip, highlighting the effectiveness of the proposed flip-flop in high-speed standard cell-based applications.

"Sense-Amplifier Based Flip-Flop With Transition Completion Detection for Low Voltage Operation,"

A novel high-speed and highly reliable sense-amplifier-based flip-flop with transition completion detection (SAFF-TCD) is proposed for low supply voltage (VDD) operation. The SAFF-TCD adopts the internally generated detection signal to indicate the completion of sense-amplifier stage transition. The detection signal gates the pull-down path of the sense-amplifier stage and the slave latch, thus overcoming the operational yield degradation, current contention, and glitches of previous SAFFs. The operational yield, speed, hold time, energy consumption, and area of the proposed and previous FFs are quantitatively compared for a wide range of VDD with 22-nm FinFET technology. It is shown that the minimum VDD of the SAFF-TCD is 573 mV lower than that of previous SAFFs, which means the SAFF-TCD can operate even when VDD is in the near-threshold or subthreshold region. At 0.3-0.4 V, the SAFF-TCD operates twice as fast as the master-slave-based FF (MSFF) with a practical hold time. Even with these benefits, the energy consumption overhead is limited to less than 20% compared with that of MSFF, and the area is similar to that of previous SAFFs.

"An Ultra-Low-Power Fully-Static Contention-Free Flip-Flop With Complete Redundant Clock Transition and Transistor Elimination,"

A redundancy eliminated flip-flop (REFF) is proposed targeting wide-range voltage scalability (1–0.3 V). Two types of redundancies are eliminated in the REFF to achieve low-power (LP) and reliable operation even in the sub-threshold voltage regime. First, redundant internal clock transitions are eliminated without degrading reliability by finding the optimal way of generating internally inverted clock to reduce dynamic power consumption. Then redundant transistors are identified and eliminated with a topological and logical method while keeping it fully static and contention-free. The simulation results show that the REFF is currently the only FF that

fully eliminates redundancy while maintaining static and contention-free operation, and is reliable down to 0.31 V in Monte-Carlo simulations. The measurement results from a test chip fabricated in 28-nm LP CMOS technology show that the measured power is reduced by 69.7%/58.7% with 0%/10% activity at 1 V and by 70.3%/58.2% with 0%/10% activity at 0.4 V compared to the conventional transmission gate flip-flop (TGFF). A total of 100 dies from five corners were tested to demonstrate the reliability, and the REFF was functional down to 0.28 V.

A Fully Static True-Single-Phase Clocked Dual-Edge-Triggered Flip-Flop for Near-Threshold Voltage Operation in IoT Applications

A Dual-Edge-Triggered (DET) flip-flop (FF) that can reliably operate at low voltage is proposed in this paper. Unlike the conventional Single-Edge-Triggered (SET) flip-flops, DET-FFs can improve energy efficiency by latching input data at both clock edges. When combined with aggressive voltage scaling, significant efficiency improvement is expected. However, prior DET-FF designs were susceptible to Process, Voltage and Temperature (PVT) variations, limiting their operation at low voltage regimes. A fully static true-single-phase-clocked DET-FF is proposed to achieve reliable operation at voltages as low as a near-threshold regime. Instead of the two-phase or pulsed clocking scheme in conventional DET-FFs, a True-Single-Phase-Clocking (TSPC) scheme is adopted to overcome clock overlap issues and enable low-power operation. Fully static implementation also enables robust operation in a low voltage regime. The proposed DET-FF is designed in 28nm CMOS technology, and a comprehensive analysis including post-layout Monte Carlo simulation for wide PVT ranges is performed to validate the design approaches. Extensive analysis and comparison with prior-art DET-FFs confirmed that the proposed DET-FF can operate at the lowest voltage of 0.28 V for a temperature range of -40 °C to 120 °C while maintaining nearly-best energy efficiency and power-delay-product.

III. EXISTING METHOD

SENSE-AMPLIFIER-BASED FLIP-FLOP

CONDITIONAL BRIDGING

To resolve issues related to the shorting device (M4) in conventional SAFFs in a more power-efficient manner, a conditional bridging technique is proposed. It is inspired by the fact that, in order to eliminate relevant redundant transitions completely, the shorting device should be turned on only when D changes after being captured by Q. In other cases, the device is better turned off to avoid the burden of using a weak device and to prevent the internal node (X or Y) on the opposite branch from being redundantly discharged. The SA stage with a circuit for supporting the conditional bridging is shown in FIGURE 4, where the output (CBG) of the circuit drives the shorting device. The proposed conditional bridge circuit makes M4 turned on during CK=1 only when D changes and becomes different from Q by monitoring the values of D, DB, SB, and RB. When CK is low, CBG is kept low regardless of the D value since SB and RB are

precharged high, turning M13, M17, and one of M12 and M16 on. At the rising clock edge, SB or RB discharges according to the value of D. If SB is assumed to be discharged, D =RB=1 allows CBG to stay low by M16 and M17. If D changes to low, CBG goes high by M14 and M15, letting M4 be turned on to provide a DC path to the ground, ensuring static operation.

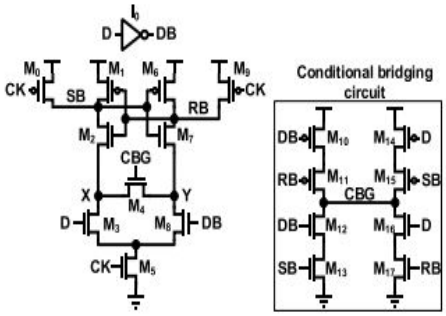


FIGURE 4. The SA stage with conditional bridging circuit.

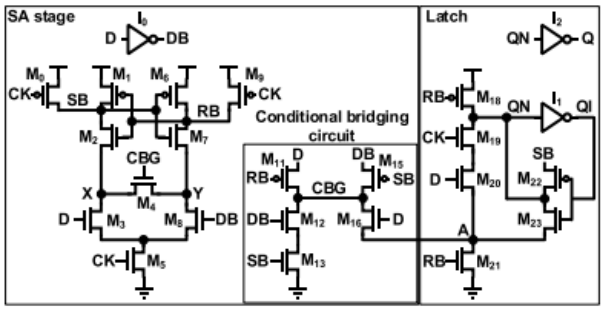


FIGURE 5. Single-ended version of the proposed flip-flop.

STRUCTURE AND OPERATION

Adopting the conditional bridging technique described above, two versions of the proposed conditional-bridging flip-flop (CBFF) are proposed. FIGURE 5 depicts the single-ended version (CBFF-S) composed of a senseamplifier stage (M0-M9 and I0) with the conditional bridging circuit (M11-M16) and a single-ended latching stage (M18- M23, I1, and I2). The conditional bridging circuit is modified to reduce the total number of transistors in the flip-flop. Specifically, the sources of M11 and M15 are directly driven by D and DB, respectively. M17 driven by RB in FIGURE 4 is merged with M21 in the latch in FIGURE 5. For letting the latching stage be optimized in terms of power consumption and device count, the glitch- and contention-free single-ended latch driven by the SA stage with no inversion is used, as shown on the right part in FIGURE 5. The pull-up and pull-down of QN after the rising clock edge are performed by M18 and M19-M21 utilizing only RB, respectively. The insertion of M20 driven by D is to eliminate glitches on QN due to the precharged high value of RB at the start of the clock high-period. SB is used for driving the source of M22 to let QN be pulled down with no contention. The source of M23 is also connected to node A to let QN be pulled up without contention. Note that the latching stage of CBFF-S in FIGURE 5 is different from traditional pulsed latches [13], [14], [15] because no pulsed operation is involved. CBFF-S has advantages in terms of power consumption, latency, and operational reliability. Letting the shorting device (M4) be turned on only when it is necessary by the control of the conditional bridging circuit can totally eliminate redundant transitions on CBG. Since the transition of CBG happens when D changes after Q captures D

during CK=1, adopting the conditional bridging circuit will result in a substantial power reduction, especially at low switching activities [22], [23]. The circuit also resolves the issue of weakening the shorting device so that the device can be sized minimum, resulting in further power reduction. Another reason for the reduced power consumption of CBFF-S comes from the fact that the opposite precharge node (X or Y) is discharged only when D changes, which is rare at a typical low input switching activity. As mentioned earlier, in conventional SAFFs, they are precharged and discharged every clock cycle. As for the speed, the reduced parasitic capacitance relevant to the shorting device whose size is the minimum allows the timing-critical signals like SB and RB to be pulled down faster, contributing to lowering the latency. A complete turnoff of the shorting device prevents the signal fighting between SB and RB during the input sampling, further improving the speed. To minimize the clock-to-output (CQ) latency, the latching stage is designed to be directly driven by RB without signal inversion and contention, as mentioned earlier. Completely eliminating the contention in the SA stage can also provide a reliable pull-down of precharged nodes at a low supply voltage region. Composed of the conditional-bridging SA stage and the contention-free latching stage allowing the output to reliably capture input data, CBFF-S can offer a stable operation down to the NTV region where variability is large. The differential version (CBFF-D) of the proposed flip-flop is shown in FIGURE 6. Thanks to the symmetric differential structure, the conditional bridging circuit can avoid one more transistor (M13 in FIGURE 5) by letting it be merged with M30 in FIGURE 6. In the latching stage, for letting differential outputs Q and QB be directly driven by SB and RB, respectively, some transistors are added with the output inverter (I2 in FIGURE 5) removed. To improve the pull-down speed of outputs by preventing the fighting against pull-up keeper transistors M22 and M25, M24 driven by CK is inserted in series with them. Although a circuit structure similar to one in the single-ended version (M22 driven by SB in FIGURE 5) is effective at nominal supply voltage, our Monte-Carlo simulation result indicates that a reliability issue can happen at worst corners, so a method of inserting a clocked transistor (M24) is used. CBFF-D has almost all the features of its single-ended counterpart, sharing the advantages of reduced power and improved speed. Although the overall power consumption of CBFF-D may be somewhat larger than CBFF-S due to the larger load capacitance of CK for driving the differential latch, its power reduction feature is still valid among differential flip-flops when switching activity is low majorly due to the conditional bridging operation. The speed of CBFF-D will be faster than CBFF-S since the differential outputs of latch, Q and QB, are directly driven in parallel by the outputs of the SA stage.

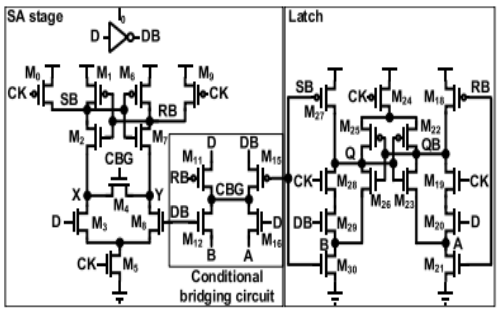


FIGURE 6. Differential version of the flip-flop.

In general, the setup and hold times can be obtained by finding the time points where Q cannot capture D by sweeping the input arrival time [14]. Then, the setup-hold window representing the minimum required input pulse width can be written as Tinput_width = Tsetup + Thold (1) where Tsetup, Thold , and Tinput_width are the setup and hold times and the minimum input pulse width, respectively. These timing parameter values of the proposed flip-flops are similar to the conventional SAFFs because they have similar SA stage structures for sampling the input data. The minimum DQ latency can be obtained by sweeping the input arrival time to find the minimum time difference between input arrival and the corresponding output change and can be written as TDQ_min= min{TD−CK (ta) + TCQ(ta)} (2) where min{a} finds the minimum value among all possible values of a. TD−CK (ta) and TCQ(ta) are the time difference from a valid input change to the corresponding clock transition, and the CQ latency at the given input arrival time ta, respectively. From (2), we can surmise that a lower minimum DQ latency of the proposed flip-flops can be expected by the reduction of the CQ latency resulting from the conditional bridging without contention and signal inversion. Regarding the power consumption of a flip-flop, the overall power consumption results from charging and discharging relevant node capacitances (PCH) and having the short-circuit current (PSC) and device leakage (PLK). So, the overall power consumption can be written as Pall = PCH + PSC + PLK (3) Since PCH and PSC result from signal transitions, the proposed conditional bridging technique eliminating the redundant transitions and reducing the parasitic capacitances at internal nodes will result in the overall power reduction of the proposed flip-flops.

IV. PROPOSED METHOD

CONDITIONAL-BOOSTING FLIP-FLOP:

For incorporating the conditional boosting into a precharged differential flip-flop, four different scenarios regarding input data capture should be considered, which are determined by the logic states of the input and output. These scenarios are as follows:

1) for a low output data, a high input data should trigger boosting for a fast capture of incoming data;

2) for a low output data, a low input data should trigger no boosting since the input need not be captured;

3) for a high output data, a low input data should trigger boosting for a fast capture of incoming data;

4) for a high output data, a high input data should trigger no boosting.

These scenarios can be embodied into a circuit topology using a single boosting capacitor by a combination of two operation principles. One is that the voltage presetting for the terminals of the boosting capacitor must be determined by the data stored at the output (so-called *output-dependent presetting*). The other principle is that boosting operations must be conditional to the input data given to the flip-flop (so called *input-dependent boosting*).

The conceptual circuit diagrams for supporting these principles are shown in Fig. . To support the output-dependent presetting, the preset voltages of capacitor terminals *N* and *NB* are made to be determined by outputs *Q* and *QB* as shown in Fig. (a). If *Q* and *QB* are low and high, *N* and *NB* are preset to be low and high [left diagram in Fig. (a)], and if *Q* and *QB* are high and low, *N* and *NB* are preset to be high and low [right diagram in Fig. (a)], respectively. To support the inputdependent boosting, the noninverting input (*D*) is coupled to *NB* through an nMOS transistor and the inverting input (*DB*) is coupled to *N* through another nMOS transistor, as shown in Fig. (b). Then, as one case in which a low data is stored in the flip-flop, resulting in the capacitor presetting given in the left diagram in Fig. (a), a high input allows *NB* to be pulled down to the ground, letting *N* being boosted toward –*VDD* due to capacitive coupling [upper left diagram in Fig. (b)]. Meanwhile, a low input allows *N* to be connected to the ground, but since the node is already preset to *VSS*, there is no voltage change at *NB*, resulting in no boosting [lower left diagram in Fig. (b)]. As the other case in which a high data is stored in the flip-flop, resulting in the capacitor presetting given in right diagram in Fig. (a), a low input allows *N* to be pulled down to the ground, letting *NB* being boosted toward –*VDD* due to capacitive coupling [lower right diagram in Fig. (b)].

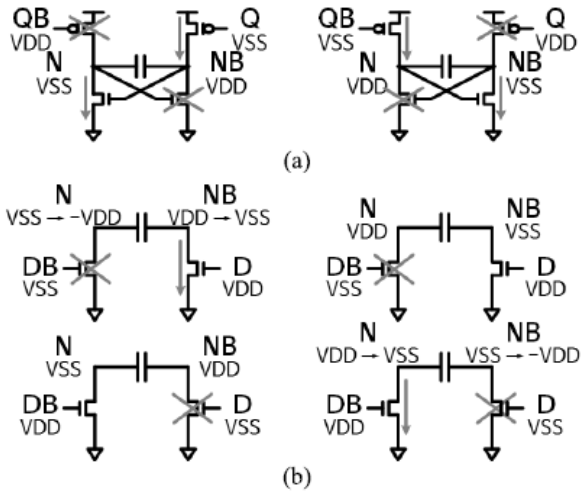


Fig. . Conceptual circuit diagrams for (a) output data-dependent presetting and (b) input data-dependent boosting

TABLE I
DATA-DEPENDENT PRESETTING AND BOOSTING

	input (D)	output (Q)	boosting node (N)	boosting node (NB)
output-dependent presetting	-	VSS	VSS	VDD
		VDD	VDD	VSS
input-dependent boosting	D=VDD	VSS	VSS → –VDD	VDD → VSS
		VDD	VSS	VDD
	D=VSS	VSS	VDD	VSS
		VDD	VDD → VSS	VSS → –VDD

Meanwhile, a high input allows *NB* to be connected to the ground, but since the node is already preset to *VSS*, there is no voltage change at *N*, resulting in no boosting [upper right diagram in Fig. 1(b)]. Table I summarizes these operations for easier understanding. With these operations, any redundant boosting can be eliminated,

resulting in a significant power reduction, especially at low switching activity.

The structure of the proposed conditional-boosting flip-flop (CBFF) based on the concepts described in the previous section is shown in Fig. 2. It consists of a conditional-boosting differential stage, a symmetric latch, and an explicit brief pulse generator. In the conditionalboosting differential stage shown in Fig. (a), MP5/MP6/MP7 and MN8/MN9 are used to perform the output-dependent presetting, whereas MN5/MN6/MN7 with boosting capacitor *C*BOOT are used to perform the input-dependent boosting. MP8–MP13 and MN10–MN15 constitute the symmetric latch, as shown in Fig. (b). Some transistors in the differential stage are driven by a brief pulsed signal *PS* generated by a novel explicit pulse generator shown in Fig. (c). Unlike conventional pulse generators, the proposed pulse generator has no pMOS keeper, resulting in higher speed and lower power due to no signal fighting during the pull-down of *PSB*. The role of the keeper to maintain a high logic value of *PSB* is done by MP1 added in parallel withMN1, which also helps a fast pull-down of *PSB*. At the rising edge of *CLK*, *PSB* is rapidly discharged by MN1, MP1, and I1, letting *PS* high. After the latency of I2 and I3, *PSB* is charged by MP2, and so *PS* returns to low, resulting in a brief positive pulse at *PS* whose width is determined by the latency of I2 and I3. When *CLK* is low, *PSB* is maintained high by MP1, although MP2 is OFF. According to our evaluation, the energy reduction is up to 9% for the same slew rate and pulse width.

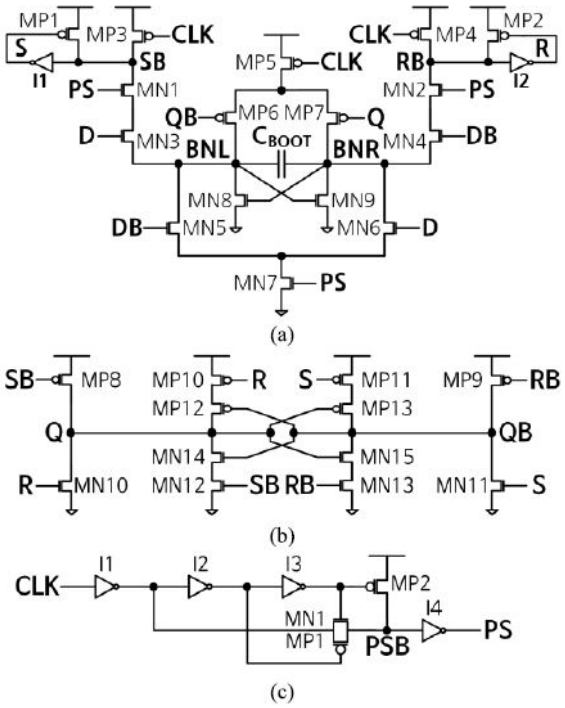


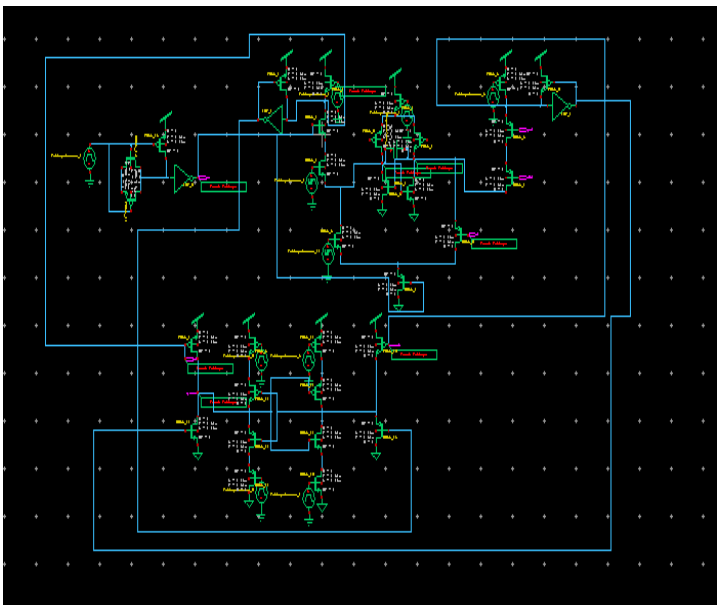
Fig.. Proposed CBFF. (a) Conditional-boosting differential stage. (b) Symmetric latch. (c) Explicit brief pulse generator

To explain the operation, let us assume that initially *Q* is low when *CLK* is low. Then, *BNR* is preset high due to the turn-ON of MP5 and MP7, and *BNL* is preset low due to the turn-ON of MN8 (outputdependent presetting). Now, when *PS* becomes high after the rising edge of *CLK*, *BNL* (*BNR*) will be connected to either *SB* (*RB*) or *VSS* depending on the input data. As shown in the first cycle in Fig. 3, since *D* is high (different from *Q*), *BNR* is pulled down to *VSS* through MN6 and MN7, and *BNL*, which is connected to *SB* through MN1 and MN3, becomes lower than *VSS* by the capacitive coupling through *C*BOOT (input-dependent boosting). This operation results in an increased driving strength of MN1 and MN3 and a fast pull-down of *SB*. A slight forward body bias established by the negative voltage at *BNL*

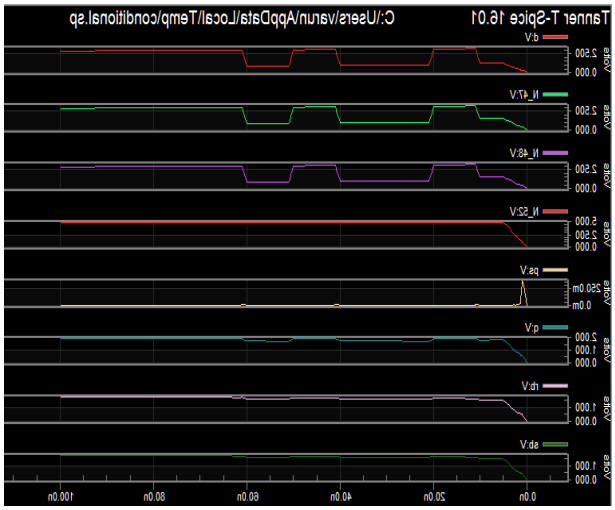
reduces the *V*TH and plays a role in further increasing the driving capability. Moreover, the negatively boosted voltage transferred to *SB* allows the pMOS transistor in I1 and MP8 in the symmetric latch to have an increased driving capability, resulting in a fast pull-up of *Q*. Although the boosted *SB* becomes briefly floating after the pull-down of *PS*, any possible rise of *SB* due to leakage never causes output flipping, because MP13 and MN14 in the symmetric latch are fully OFF. Due to this condition, thecircuit may not be adequate for operations at extremely low frequency. At the following falling *CLK* edge, *BNL* is preset high through MP5 and MP6 because now *QB* is low, letting *BNR* be preset low through MN9 (output-dependent presetting). *SB* is also precharged high by MP3. As implied by the operation described above, the latency of the proposed flip-flop is substantially reduced by voltage boosting that increases the driving strength of transistors. Enlarged gate-source voltage of transistors along the timing-critical paths contributes to this feature. A slightly forward source-body voltage established in some of these transistors by boosting source voltages below the ground leads to a reduction in threshold voltages, further increasing the driving strength. Since an increased *V*GS and a decreased *V*TH implies an increased effective voltage (*V*GS-*V*TH), process variations cause less latency variation, resulting in decreased performance variability. Moreover, based on the proposed output-dependent presetting and input-dependent boosting, boosting is done only when the input data is different from the stored one, resulting in the conditional boosting operation. Thus, large power-consuming redundant boosting operations can be eliminated, resulting in a substantial improvement in energy efficiency especially at low switching activity. The soft-edge property provided by the pulsed operation improves tolerance to clock skew and clock jitter and enables time-borrowing. Since the pulse can be shared among multiple flip-flops, the energy consumed by the pulse generator can be reduced. To lower the energy overhead due to explicit pulse generation, a novel brief pulse generator is designed. Although the proposed flip-flop is based on voltage boosting where some internal node voltages go beyond the supply voltage, they cause no overstress problem, because they target the near-threshold operation where the maximum voltage including the boosted level is still less than 1

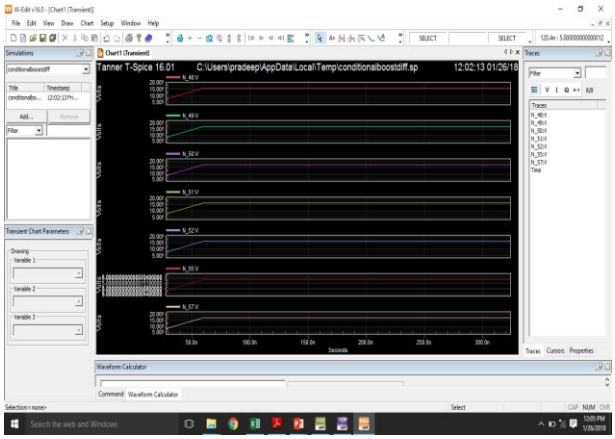
V.RESULTS & SIMULATION

SCHEMATIC



SIMULATION RESULTS





AREA AND DELAY

```
Device and node counts:
             MOSFETs -      37
    MOSFET geometries -       3
          Capacitors -       1
      Voltage sources -      10
          Subcircuits -       3
    Model Definitions -       2
      Computed Models -       2
    Independent nodes -      57
       Boundary nodes -      11
          Total nodes -      68
*** 11 WARNING MESSAGES GENERATED DURING SETUP


Parsing                     0.02 seconds
Setup                       0.03 seconds
DC operating point          0.36 seconds
Transient Analysis          0.05 seconds
Overhead                    0.25 seconds
-----------------------------------------
Total                       0.70 seconds
```

VI. CONCLUSION

For forceful voltage downsizing to the close limit voltage locale without serious execution debasement, a novel CBFF has been proposed. A heartbeat activated FF plan for low power applications utilizing lift body driven plan is exhibited in this venture. At long last, a multibit flipflop idea is presented with contingent boosting flipflop for productive improvement of intensity zone and postponement.

For aggressive voltage scaling down to the near-threshold voltage region without severe performance degradation, a novel CBFF has been proposed. A pulse triggered FF design for low power applications using boost body driven scheme is presented in this project. Finally, a multibit flipflop concept is introduced with conditional boosting flipflop for efficient improvement of power area and delay

VII. REFERENCES

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